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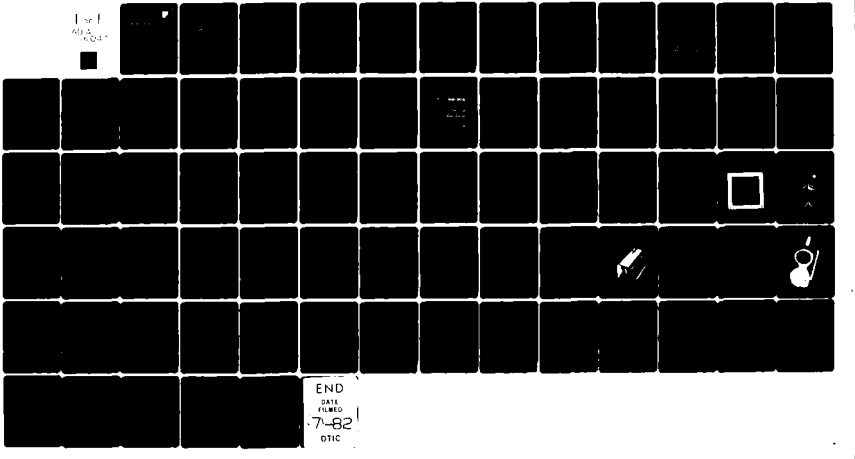

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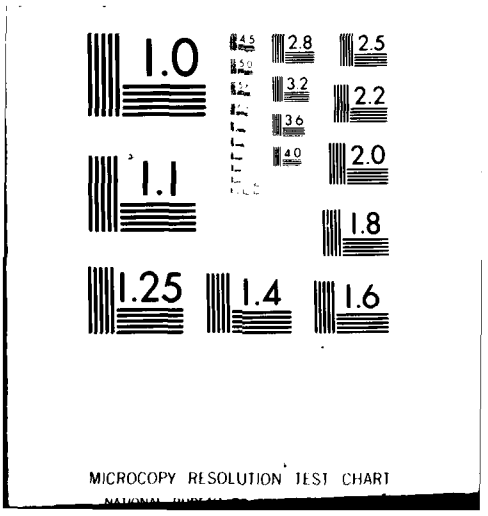
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RADC-TR-82-57
Final Technical Report
March 1982

A COMMUNICATIONS OPTICAL PROCESSING TECHNIQUE

Naval Ocean Systems Center

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This report describes the development and test of an incoherent electro-optical processor. This processor was developed to demonstrate the utility of this device as an incoherent E-O processor, as a high speed, high resolution discrete Fourier transform device. The processor is being developed to analyze multiple communication channels simultaneously.

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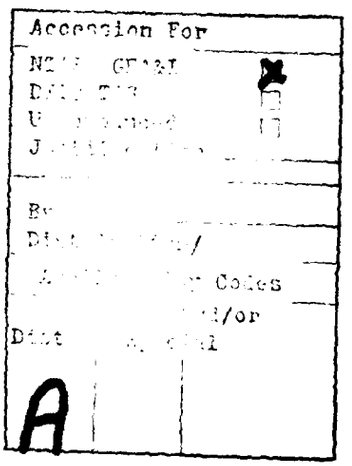

1.0 INTRODUCTION

1.1 BACKGROUND

An electro-optical method for performing analog signal processing operations using the inherent fast matrix multiplication of incoherent optical systems has been under development at NOSC over a period of years.[1,2,3] The reader who is unfamiliar with this device is referred to reference 2 and 3 for a complete description of its concept of operation and application areas. The strengths of this implementation are its small size (a few cubic inches), its low power (<5 watts), its potential low cost (<$1k), its broad applicability (the computation of any discrete linear transformation), and its very high speed (input rates of several Megahertz). The device is called an electrooptical processor (EOP) and its essential components, shown in Fig. 1.1, are as follows:

a. A high speed real-time modulated light source consisting of a light-emitting diode (LED),

b. An optical memory matrix consisting of a pattern of apertures having a range of transmissivities. Each aperture is associated with one element (pixel) of a two-dimensional photosensing array, in most cases a charge coupled device imager (CCD),

c. A CCD capable of integrating the charge generated by a series of light pulses so that summing operations can be performed. Because such imagers contain a large number of parallel registers, many summing operations can be performed simultaneously. A serial readout of one row from the array of column registers is required as an integral part of the device.

The EOP performs matrix-vector products of the form

$$g_m = \sum_{n=1}^{N} f_n \, h_{m,n}$$

where f_n is the sequence of analog samples of the input data and $h_{m,n}$ is a fixed predetermined matrix. The multiplications required for this operation occur as light from the LED, modulated by the input signal f_n, passes through

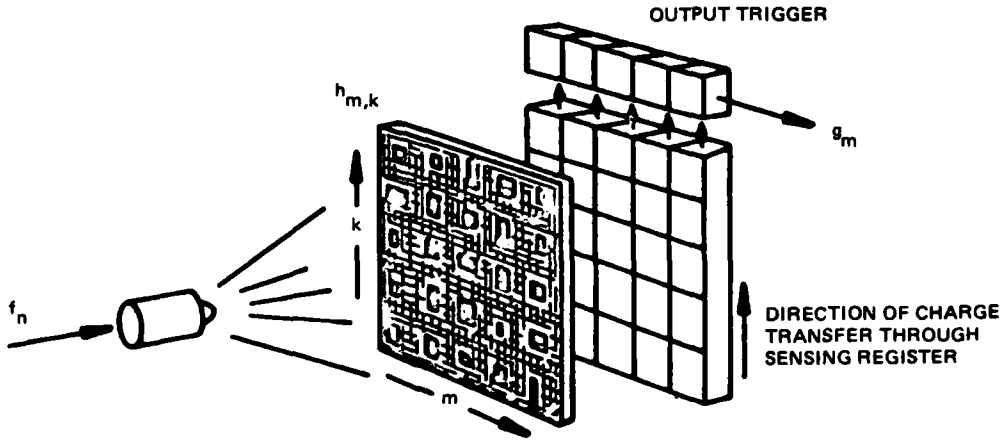

Figure 1.1. Basic components of the Electro-Optical Processor System.

the partially transparent mask containing the matrix $h_{m,n}$ as its transmittance function. The intensity of the light emanating from the mask is indeed the product of the irradiance of the original light and the intensity transmittance of the mask. Summation occurs through the ability of the CCD to convert these photons into charge packets, with a direct linear relationship between total light impinging on a cell and the amount of charge accumulated. By shifting the charge packets upward by one resolution cell (pixel) per input sample to the LED, addition of the proper terms through the addition of these charge packets is accomplished.

Because the CCD imagers developed as the sensor for solid state television cameras share most of the fundamental characteristics required for the EOP, it has been possible to use off-the-shelf devices in carrying out the initial development and evaluation of this system.

First, all camera sensors are capable of integrating an optical input for at least one TV frame period (33 ms). Second, the architecture of frame transfer sensors permits the charge analog of a series of light pulses to be summed by coordination of light exposure and transfer of a charge packet through each column (vertical) register of the image sensing and storage

areas. The number of columns in the device determines the number of simultaneous summations that will be performed. Third, the output register takes the summed output from the last stage of each column and serially transfers these charge packets to the output stage of the device.

Incorporation of the optical memory matrix into the EOP has followed two paths. In a laboratory setup that has the flexibility for replacing either mask or sensor, a separate mask has been used which requires precision optics to align the array of apertures onto the imager. The other consists of a more rugged and compact setup which requires the aperture mask to be made integral with the CCD imager so that one particular optical memory mask is committed to each imager. There have been two NOSC contracts with RCA Laboratories directed to providing samples of RCA's SID52501 CCD Imager on which an opaque mask containing an array of apertures was fabricated.* Each aperture is centered over one pixel of the 320 x 512 pixels of the device.

The number of discrete levels or aperture weights that a processor system using these basic components is capable of handling will depend upon (1) the minimum incremental change in aperture area which can be built into the optical memory mask covering the sensor, and (2) the minimum signal increment detectable in the output from the CCD imager as determined by the noise in the output signal and the maximum charge capacity of a single pixel. Useful data is provided by the readout of that one horizontal line containing the row of integrated charge packets from a selected sequence of illuminations and transfers.

After considerable experimentation with EOP's incorporating commercially available CCD's designed for television imaging, it became readily apparent that a custom CCD, designed explicitly for use as an EOP sensor, was required. This custom device should incorporate a gate to control the transfer of charge between the array and the output register and should be optimized for dynamic range, uniformity, linearity, and speed (at the expense, if necessary, of sensitivity and broad spectral response). Such a custom device has been designed and fabricated by RCA Laboratories and has been demonstrated in an EOP at the Naval Ocean Systems Center (NOSC). The

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* Contract numbers N00123-77-C-0702 and N66001-78-C-0149.

remainder of this report details the results to-date of this effort. Chapter 2 deals with the design and fabrication of the custom gated-output CCD chips. It is extracted almost verbatim from progress reports to NOSC by RCA Laboratories. Chapter 3 discusses the design and preparation of the matrix masks which, when superimposed on the CCD, determine which transformation the EOP performs. Chapter 4 describes the computerized test system for characterization of the EOP. Chapter 5 gives the preliminary results of this characterization. Finally, chapter 6 discusses the implementation of a discrete Fourier Transform (DFT) module based upon the EOP.

2.0 THE GATED-OUTPUT CCD ARCHITECTURE

2.1 DESCRIPTION OF THE EOP PROGRAM

The purpose of this work has been to obtain and evaluate prototype samples of a customized CCD imager which, more adequately than any existing device, satisfies the specific requirements of the EOP.

2.1.1 Organization of the Gated Output CCD

This section is a report on the design, fabrication and results of tests performed by RCA in the Princeton Laboratories by Mr. Dan Cope.

The Gated-Output CCD shown schematically in Figure 2-1 was designed to meet the special requirements of the EOP type of use. It is an all-buried channel device with a two-level, overlapping polysilicon gate structure driven by two clock phases. The image area consists of 128 parallel CCD registers separated by 5 μm channel stops, each containing 128 stages with a picture element (pixel) area of 50x50 μm. As shown in this figure, the double-end connected MOS gate lines of the image registers are continuous across all 128 vertical transfer columns, so that all charge packets along a horizontal row are transferred simultaneously with each clock cycle.

In operating a conventional frame transfer imager in the EOP system, photo-generated charge packets are moved continuously through each vertical column of an array of parallel CCD registers until they reach the horizontal output register. They are then shifted one horizontal line at a time to the output stage. The only useful output signal from the device is that which represents a particular sequence of multiplications (light-intensity x aperture transmissivity) that have been summed in each column and are read out as one output row. Because all other rows read through the output must be discarded, the maximum data rate of the system is determined by the transfer frequency of the output register.

It has been apparent for some time that a desirable improvement for the CCD imager intended for EOP application would be the inclusion of a gate controlling transfer from the vertical registers into the output register. Only selected data would then be transferred to the output stage, the remainder being dumped into drain sites. The transfer frequency of the vertical registers would then determine the data sampling rate.

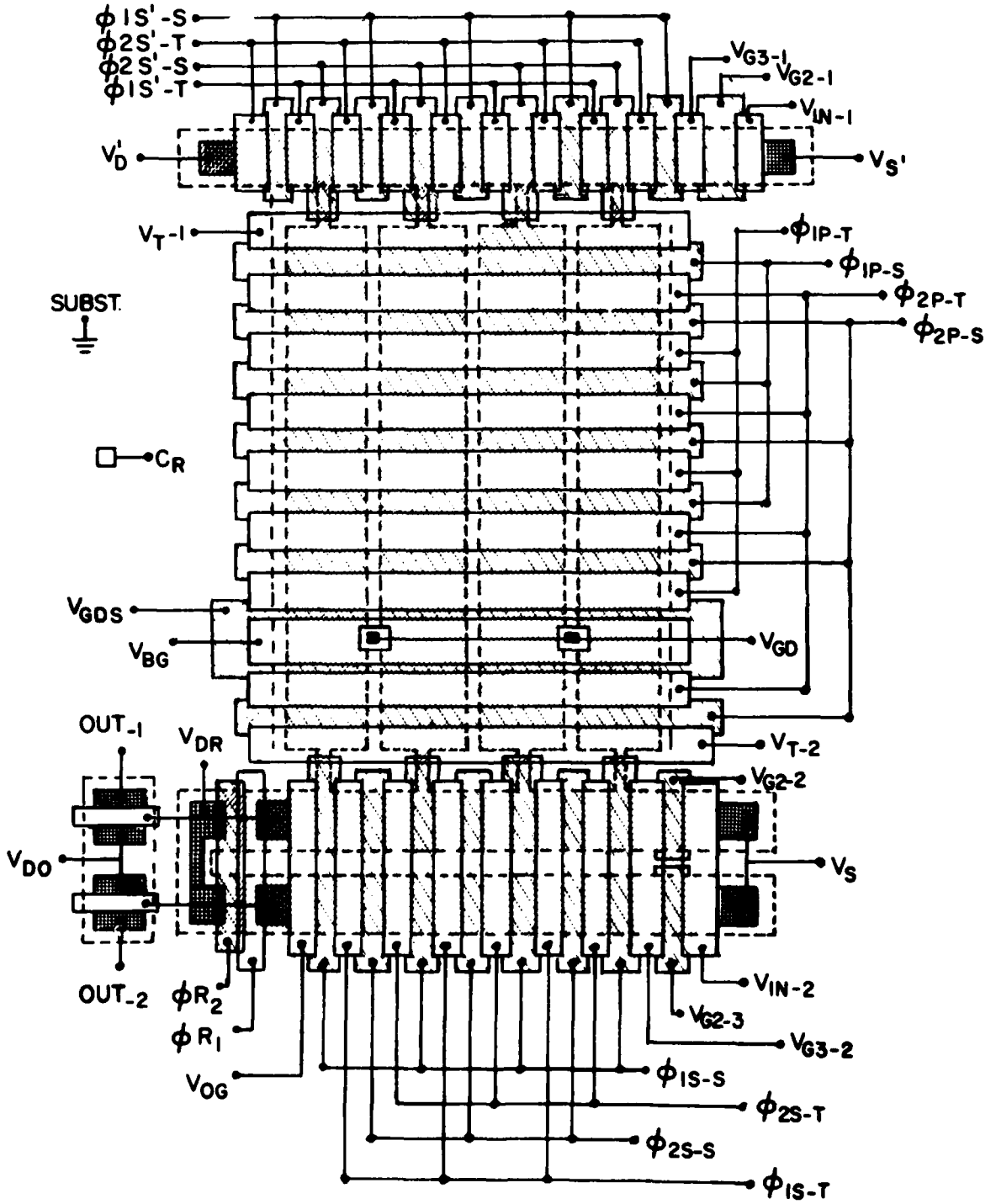

Figure 2-1. Schematic diagram of the Gated-Output CCD.

The principal innovation for the EOP gated-output CCD is a stage located between the image register and the output register having a gate that controls either the readout or dumping of a line of signal charges as they are transferred out of the vertical registers.

Other important features and operating capabilities which are design objectives for this customized device are:

a. the ability to transfer charge through the vertical registers at a frequency of 1 MHz or greater.
b. uniform photosensitivity over the vertical register array.
c. a linear relationship between the light irradiance falling on a pixel and the output voltage conversion of the photogenerated charges.
d. a large dynamic range.
e. simple driving waveforms to be applied to the CCD gates.

Fig. 2-2a shows schematically the cross-section of the polysilicon gate structure of a pixel in the image area. The first level storage gates have been made longer than the second level transfer gates in order to provide the largest possible area covered by only one thickness of polysilicon. For the signal processor application the signal is generated by light passing through the apertures in the optical memory mask. These mask openings are confined to the first level poly regions.

Fig. 2-2b shows the pixel cross-section in the output register. Here the length of the storage and transfer gates is equal. The output register is 80 μm wide.

To aid in making quantitative measurements of the device performance, or for applications other than the present EOP, an input register (shown at the top of Fig. 2-1) has been included in the design. With its "fill-and-spill" input stage[4] this register provides the means for introducing a low-noise signal into the top of the image register.

Signal charge in the image register is read out from the device by transferring vertically each row of charge packets through the image register and into the horizontal output register shown at the bottom of Fig. 2-1. The image register signal charge can either be a photo-charge image generated by incident light or signal introduced through the input register.

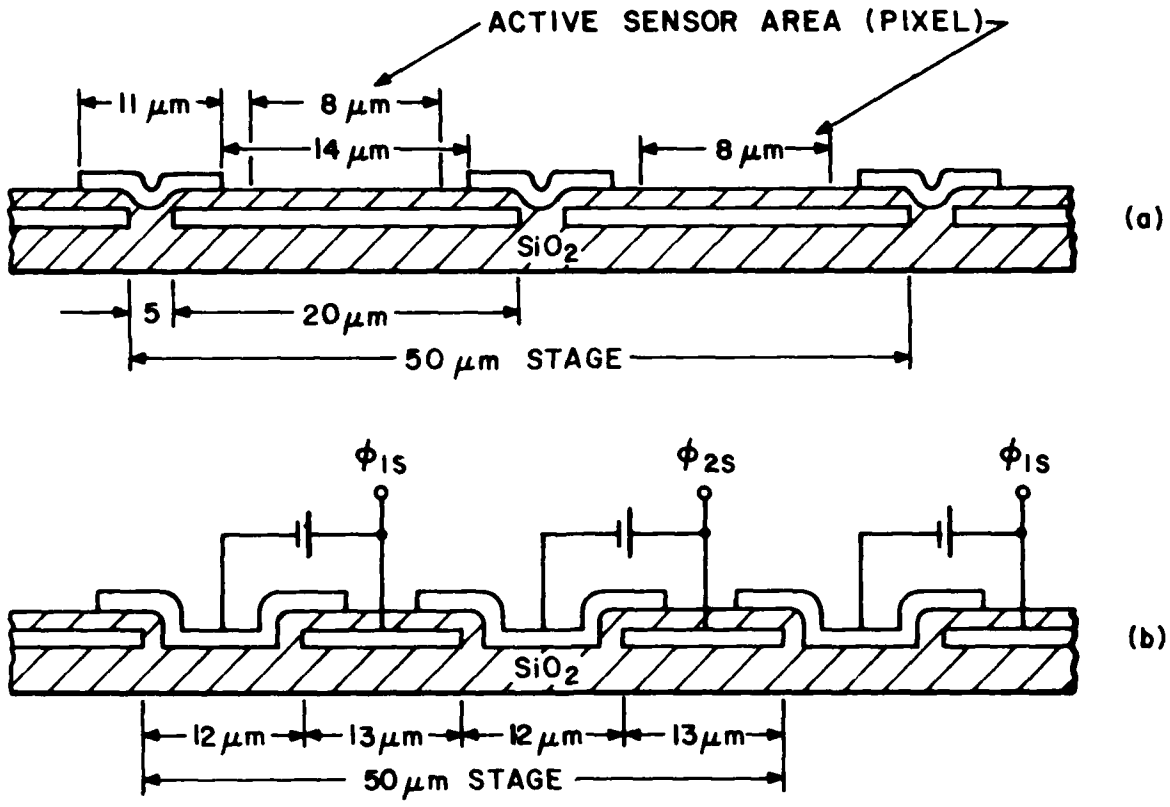

Figure 2-2. Cross-section of polysilicon gate structure of Gated Output CCD.
(a) Pixel of photosensor area.
(b) Pixel of output register.

Each row of charge packets transferred serially through the horizontal output register to the floating diffusion output stage, shown in the lower left corner of Fig. 2-1 becomes the time-varying signal fed to the off-chip amplifiers. The charges from all 128 stages of this register must be read out before a new row of charge packets can be accepted from the image area.

2.1.2 Gated-Output Stage

The particular feature of the design which makes it different from other CCD imaging structures is the gated-output stage located between the image and output registers (See Fig. 2-1). As each row of pixel charges from the image register is transferred into this stage there are two options available. The charge packets can either be transferred through to the output register, or they can be dumped into drain sites. This is an operating capability of great utility for the Electro-Optical Signal Processor when summing operations are being performed because only the occasional row containing useful output signals needs to be read out.

The structural details of the gated-output stage are shown in Fig. 2-3. It consists of a $\phi 1$ first-level polysilicon extended-length storage gate that will also be referred to as the gated-drain storage gate. It is powered by voltage pulse V_{GDS}. This first level polysilicon gated-drain storage gate contains rectangular openings (shown in dotted lines) which are covered by a second-level polysilicon barrier gate powered by voltage V_{BG}. The barrier gate also has rectangular openings that form self-aligned N+ diffusions in the substrate which are biased by voltage V_{GD}. The $\phi 2$ transfer and storage gates of this stage are of normal length. Finally, the transfer gate between $\phi 2$ of the gated-drain stage and the output register is powered by voltage pulse V_{T2}.

In the operation where the signal charge is to be transferred to the output register, the barrier gate of this gated-output stage is biased negative by voltage V_{BG} to form barriers between the $\phi 1$ storage wells and the gate-drain regions. However, if a line of signal charge is to be dumped, the barrier gate V_{BG} is biased with a more positive potential to allow the drains to act as sinks for the charge packets in the $\phi 1$ storage wells. To accommodate the drain sites and the surrounding barrier gate it was necessary to

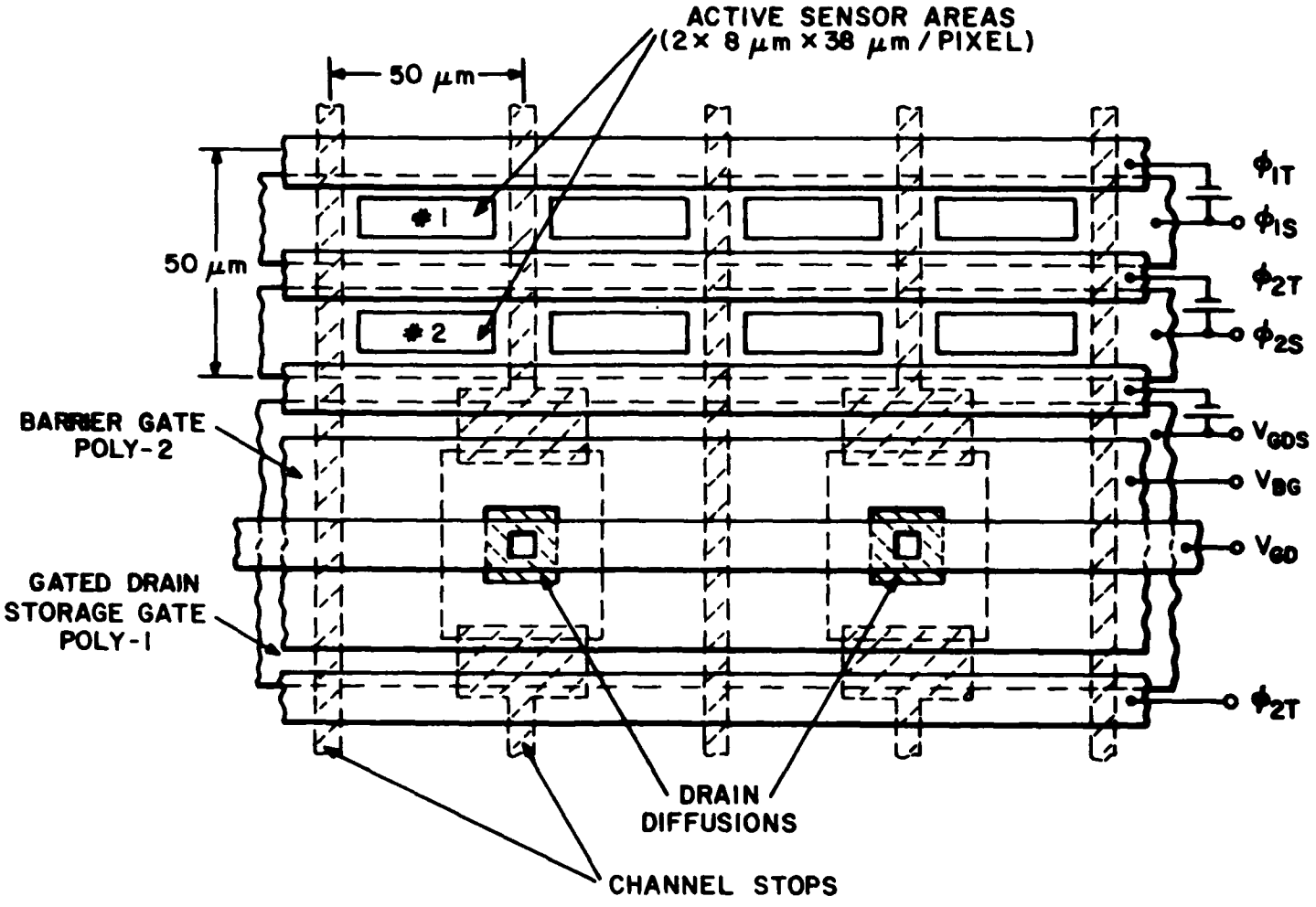

Figure 2-3. Plan view of one row of sensors of the Gated Output CCD and the details of the gated output/drain structure.

make this $\phi 1$ storage gate 1.5X longer than the other gates of the image register.

2.1.3 Noise Cancellation in Output Signal

As shown in Fig. 2-1, there is a companion to the output register which shares the same charge transfer gates but has separate input and output structures. The purpose of this dummy register, which receives no signal charge from the image register, is to permit system noise that is common to both registers to be cancelled by processing the two outputs through an operational amplifier. Past experience with CCD imaging devices has shown that this is an effective means for removing clock pulses and other fixed pattern noise from the output signal.

2.1.4 Input Stage

Fig. 2-4 is a diagram of the surface channel input stage which is a part of all three horizontal registers; the input, output, and dummy output.

The charge packet to be transferred to the register is collected in the well under V_{G2}. Charge is injected from V_S during the negative strobe interval, filling the well under V_{IN} and V_{G2}. When V_S returns to its positive value the excess charge under V_{G2} spills back to the level determined by the potential of the input signal applied to V_{IN}. The charge under V_{G2} is transferred into the register when V_{G3} and $\phi 1_S$ are pulsed positive during the ON cycle of the $\phi 1$ clock.

2.1.5 Output Stage

Fig. 2-5 is a diagram of the surface channel output stage which is part of the output and the dummy output registers. There is a separate floating diffusion for each register, but the output gate (V_{GO}) and the two reset gates (ϕR_1 and ϕR_2) are common to both.

The gate potential of the output transistor is changed by each charge packet transferred from the last $\phi 1$ stage through V_{OG} and into the floating diffusion. After the output signal has been sampled, the floating diffusion must be reset by applying a positive pulse to the negative based ϕR_2 gate. The purpose of the ϕR_1 reset gate, which is held at a constant positive bias,

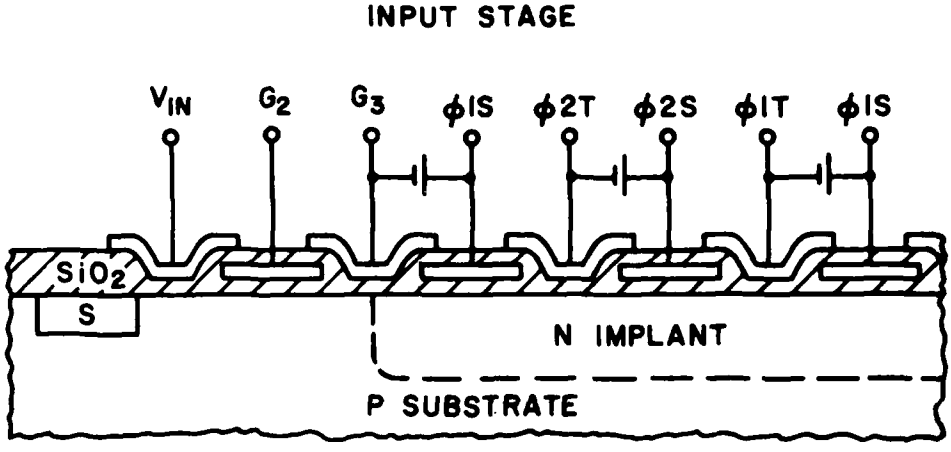

Figure 2-4. Schematic diagram of the input stage.

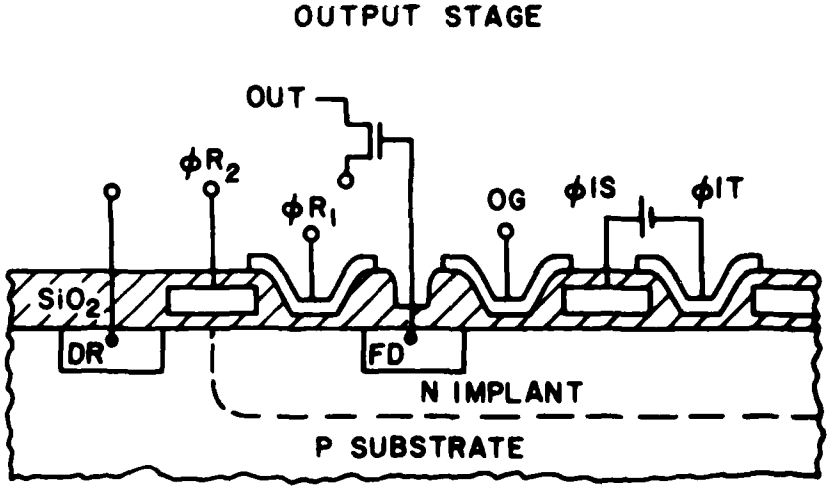

Figure 2-5. Schematic diagram of the output stage.

is to reduce the capacitive coupling of the ϕR_2 pulse into the floating diffusion.

2.1.6 Optical Memory Mask

The optical memory mask becomes an integral part of the EOSP device. It consists of an opaque layer of metal deposited on the surface of the CCD imager in which a pattern of openings has been formed. Each individual aperture is aligned with one pixel of the image register and with uniform illumination falling on the device there should be a linear relationship between the signal generated in different pixels and the area of their associated apertures. The number of aperture weights that can be used in designing the aperture pattern is determined by the dynamic range of the sensor and the minimum detectable area difference between apertures.

2.2. DEVICE FABRICATION

2.2.1 First Run Wafers

There are 9 mask levels required for fabricating the Gated-Output CCD structure. The mask set was produced on the MEBES electron beam machine of the RCA Solid State Division. The die size of .326" x .329" is repeated over the entire mask area so that when these proximity printing masks are used to pattern a 3-inch diameter substrate there are 44 complete devices per wafer. The fabrication was carried out in the Integrated Circuit Center of RCA Laboratories and the first run of ten wafers was completed in late April, 1980.

2.2.2 Selection and Packaging of Operable Devices

Each operable device on a completed wafer must be identified before the wafer is diced and the useful samples are mounted and bonded in the final package. This is done by making contact to the various electrodes using a 40-pin probe card mounted in a standard probe station. The electrode potentials and clock pulses are obtained from the same camera control and drive circuitry which is used for operating the packaged devices.

The yield of operable devices from the three wafers which have been evaluated at this time is shown in Table 2-1. The criteria for device selection at probe test were:

1) That a pulse train can be introduced through the input stage and transferred through the output register.

2) That an optical image is reproduced in the output signal without regard to cosmetic defects.

Only those devices which are capable of producing an image of reasonable quality were packaged and given more complete performance evaluation.

The operable devices are mounted in a 40-pin DIP package with a .400" x .400" chip cavity.

TABLE 2-1

Yield of Operable Devices From Three Run 1 Wafers

Wafer	Not Operable	Only Output Register Operable	Image Register Operable
A	22	4	20
B	22	16	8
C	19	14	12

2.2.3 Applying the Optical Memory Mask

After determining by probe testing that there were a number of operable devices on TC1253-1D, the optical memory mask was added to this wafer. The procedure, which had been developed in prior work with the standard SID52501 CCD Imager, consists of the following operations:

1. Over the protective oxide which covers the completed devices on the wafer a 1400A thick layer of chromium is deposited by evaporation in high vacuum. This thickness had been determined as the minimum for a fully opaque deposit.

2. Using standard photolithographic technology the area covering the image register of each device and the pattern of apertures within this area is developed in the photoresist layer covering the wafer.

   The lithographic mask containing a particular optical memory function in the form of an array of various size apertures is an additional mask level and contains the same alignment keys as the

rest of the mask set. The positioning must accurately align each aperture with the correct pixel in the underlying image register.

3. Using a standard chromium etch solution the openings are formed in the Cr covering the image register of each device and the photoresist is removed.

There is also the matter of deciding how far beyond the image area this chromium layer should extend. The boundaries of the initial electro-optical modulator mask, the test mask, were set as follows:

(1) At the sides the metal extends 10 μm beyond the edge of the first and last vertical register of the image area so that it will not overlap the inner bus bar connecting the gates of this register. This was done to avoid the possibility of bus bar short circuits. (2) At the top of the image area the metal extends over the edge of the storage gates belonging to the input register. This was done so that the potential for short-circuiting could be evaluated. Although short circuits between the chromium and these storage gates will inactivate the input register, this would not be a serious consequence since this register is not an essential feature of the electro-optical signal processor design. (3) At the bottom of the image area the metal extends to within 2 μm of the bottom edge of V_{T2}.

A chromium-covered area of this size leaves the gated-output stage and the two output registers exposed to light incident on the device. Means for shielding the device from stray light may be required.

Forming a pattern of apertures with sharply defined edges and accurate dimensions on the SID structure had been a relatively straight-forward operation because the single level gate structure produces a device with a flat outer surface. By contrast, the two-level gate structure produces a surface with ridges and valleys. As shown in Fig. 2-6 the memory mask openings must be limited to the two regions within a pixel area which are covered by only the first polysilicon level if one expects to maintain a linear relationship between the aperture weight (transmissivity) and the photo-signal. The first attempt to form an integral modulator mask on the device revealed two problems. One was poor adhesion between the deposited Cr and the oxide coating of the devices. The second was poor definition of the apertures. How readily these problems can be overcome will be determined when additional wafers are Cr coated and patterned.

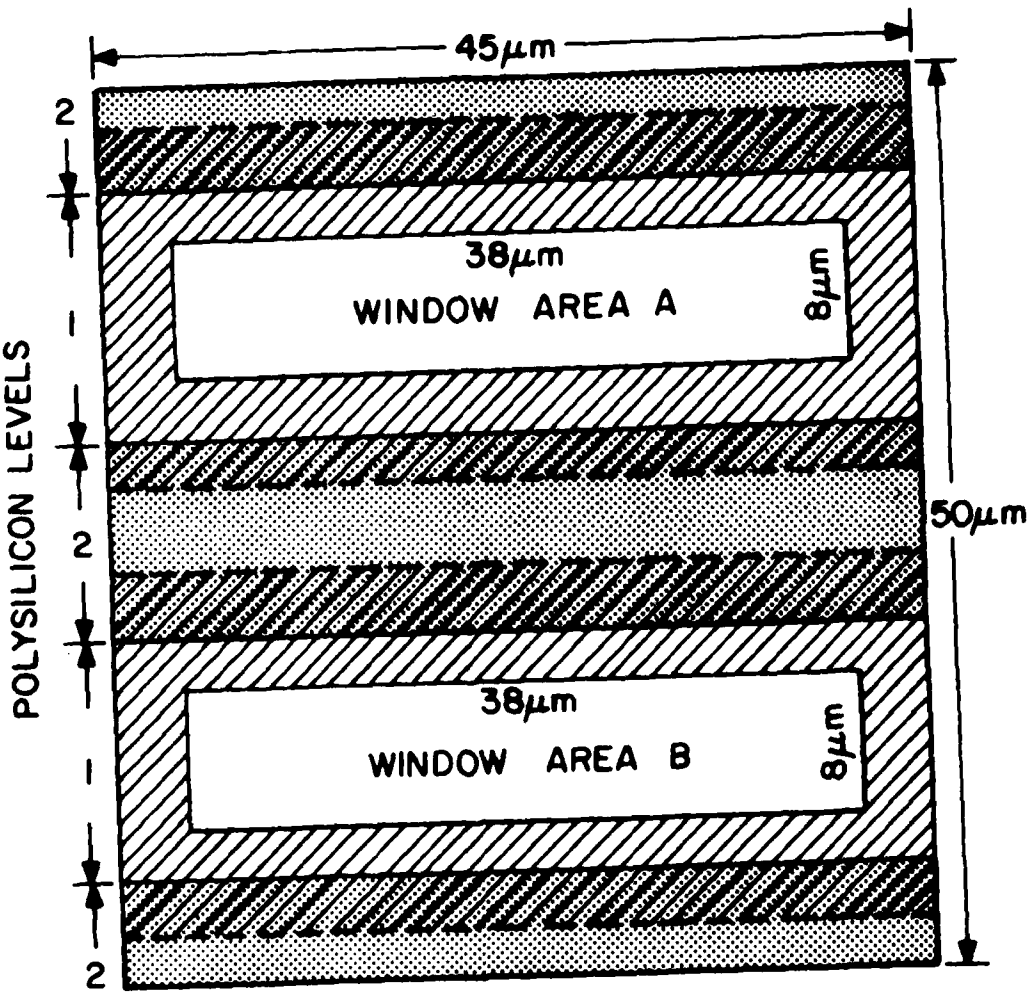

Figure 2-6. Plan view of image area pixel showing the two optical window areas.

The particular optical memory mask pattern was provided by NOSC. Four additional aperture sequences were added to the original design to provide a means to evaluate the useful dynamic range and the linearity of the transfer function relating aperture size and signal amplitude. Table 2-2 lists the dimensions of the apertures in these two sequences.

TABLE 2-2

Aperture Sequences for Test Mask

SEQUENCE I	One Horizontal and One Vertical
Pixels 1-76	In window Area A Vertical: Constant 8 μm Horizontal: Starting with 0.5 μm increase width by 0.5 μm increments to full 38 μm width.
Pixels 77-103	Starting in window area A, ending in A and B Horizontal: Constant 10 μm Vertical: Start with 3 μm in A and increase by 1 μm increments to 29 μm vertical dimension across A, the gap, and B
SEQUENCE II	One Horizontal and One Vertical
Pixel 1-76	In window areas A and B Vertical: Constant 8 μm Horizontal: Starting with 0.5 μm increase width by 0.5 μm increments to full 38 μm width
Pixel 77-84	In window area A Horizontal: Constant 1 μm Vertical: Start with 1 μm and increase by 1 μm increments to 8 μm
Pixel 85-91	In window area A Horizontal: Constant 2 μm Vertical: Start with 2 μm and increase by 1 μm increments to 8 μm
Pixel 92-98	In window areas A and B Horizontal: Constant 2 μm Vertical: Start with 2 μm and increase by 1 μm increments to 8 μm

2.3 DEVICE OPERATION AND PERFORMANCE CHARACTERISTICS

2.3.1 Operating Cycle

The initial evaluation of the devices at RCA Laboratories was made using an operating cycle which would permit the video output to be displayed on a standard TV monitor without modification of its deflection circuit. The camera control circuitry and clock drivers uses TTL logic to establish the inter-relation of the various cyclic functions.

The readout time of the 128 stage output register can be no greater than 60 μs and has usually been 30 μs (5 MHz clock). The output register is read every 60 μs, the time required for the monitor kinescope to complete its horizontal sweep. The transfer of a row of charge packets from the image to the output register takes place during the horizontal retrace time of the monitor. The clocking of the image register and the gated output stage is asymmetrical with the ON time of the $\phi 2$ gates being 10X longer than the ON time of the $\phi 1$ gates. This provides the maximum integration time for collecting the photogenerated charge in the well formed under one gate. The image register clock runs continuously, but the projected optical image is strobed only once each 1/60 second so that the image information is read out and displayed on the monitor in 129 line times and then for another 129 line times there is no video output. On the monitor the displayed output from the CCD occupies only one quarter of the raster area; half the width and half the height.

With this operating cycle the output signals from the device have been observed on the monitor display for the following conditions:

1. A train of signal pulses introduced through the input stage of the output register.
2. An image display generated by a strobed light image incident on the image register.
3. A train of signal pulses introduced through the input stage of the input register.
4. The removal (dumping) of selected rows of signal information from the image register by modulation of the gate-controlled output stage.

5. A train of signal pulses introduced through the input stage of the dummy output register.
6. Partial cancellation of fixed pattern noise when processing the signals from the two output registers through a differential comparator scope amplifier.

The limited amount of noise cancellation observed in the initial tests is the result of poor layout of the output circuitry for the two registers. Careful matching of the lead lengths, etc. is necessary in order to achieve the full capability of this operation.

Table 2-3 gives the typical voltages used for operating the devices from the first fabrication run.

These various operating exercises are evidence that every part of the design operates as intended and it is concluded that no modification of the present mask set is required.

TABLE 2-3

Typical Operating Voltages for TC1253 Devices from Run 1

Output and Dummy Output Register

V_S		12V dc with 10V negative strobe
V_{IN-2}		8V with negative signal
V_{G2-2}, V_{G2-3}		8V
V_{G3-2}		2V dc + 15V positive strobe
$\phi 1S_s$	High	10V
$\phi 2S_s$	Low	0
$\phi 1S_T$	High	5V
$\phi 2S_T$	Low	-5V
V_{DO}		15V
V_{DR}		12V
V_{R2}	High	8V
	Low	-6V
V_{R1}		6V
V_{OG}		1V

TABLE 2-3 (continued)

Image Register

$\phi 1P_s$, $\phi 2P_s$	High	10
	Low	0
$\phi 1P_T$, $\phi 2P_T$	High	5
	Low	-5
V_{GD}		12
V_{BG}	Dump	6
	Low	6
V_{GDS}		0 + $\phi 1P_s$
V_{T2}	High	5
	Low	-5

Input Register

V_s'		12V dc with 10V negative strobe
V_{IN-1}		8V with negative signal
V_{G2-1}		8V
V_{G3-1}		2V dc plus 15V positive strobe
$\phi'S'$, $\phi 2S'_s$	High	10V
	Low	0
$\phi 1S'_T$, $\phi 2S'_T$	High	5V
	Low	-5V
V_{T1}	High	3V
	Low	-5V
V_D'		15V

2.3.2 Performance Characteristics

The readout of a pulse train fed into the output register is delayed 60 μs (30 μs transfer time plus 30 μs waiting time) whereas the delay increases to 8 ms when the same pulse train is introduced into the input register. The one field delay is the time required for a signal to make a complete transit through the device (128 horizontal and 130 vertical transfers). No measureable transfer loss can be observed in signals transferred through the 128 stage buried channel CCD lines when this device is operated at the clock frequencies discussed in Section 2.3.1.

In an effort to determine the effect of increasing the clock frequency applied to the gates of the image register the following test was performed. The normal 6 μs ON time for the $\phi 1$ gates can be considered half of a 12 μs period clock (83.3 kc frequency). While noting the vertical resolution reproduced from a test pattern as this $\phi 1$ ON time is made a smaller fraction of the total clock cycle, one can arrive at an estimate of the maximum clock frequency which might be used. An equivalent clock frequency of 5 MHz was reached before any degradation in resolution was seen. At this same clock frequency the pulse shape had become distorted and the drivers could no longer maintain the full amplitude even though load resistors and capacitance had been removed from the circuit. It is not clear just how much the CCD is limiting the performance at this frequency. It appears certain, however, that operating the image register gates at a clock frequency of 5 MHz or greater would require a redesign of the drive circuits and mounting them as close as possible to the device.

The utility of a CCD imager in the Electro-Optical Signal Processor application is premised on the ability to obtain wide dynamic-range analog output signals which have a minimal spurious signal content. This requirement is no different from that for the imagers intended for use in a television camera. RCA Laboratories, in conjunction with the Electro Optics Devices group of the Solid State Division, has carried out an intensive investigation into the origins of the various classes of defects found in the SID52501 imager.[5] This involved locating in the image or storage area of the device the site responsible for a particular point, area, or line blemish as seen in the displayed video image, and then determining the specific mechanism responsible for either the injection or spurious charge or the loss of signal.

In the video display of a white field output signal from a CCD, the contrast of a blemish can vary between the extremes of a full amplitude white signal to a zero signal black. Blemishes have been observed whose contrast with respect to the surrounding background varies with operating voltage, illumination intensity, and illumination wavelength. Some exhibit voltage or illumination thresholds.

The defects originating from spurious pinholes in masking oxides or structural errors in the conducting layers of the superstructure are the more

easily identified and can be eliminated by attention to the techniques of LSI fabrication. Those defects originating within the substrate are less easily understood and controlled, in large part because a greater number of edge dislocations, micro-precipitates and local sites with a high density of recombination centers are present than ever become electrically active. An important conclusion from the step-by-step evaluation of the manufacturing process is that the decoration of defects is not the result of contamination introduced from outside, but rather is the result of a redistribution of what was present in the original wafer. In the undepleted regions of the substrate where photogeneration of carriers takes place, substrate inhomogeneities modify carrier lifetime. Blemishes in the displayed image showing contrast which varies with illumination intensity and wavelength are exhibiting behavior which is sensitive to lifetime modulations in the substrate.

The device operating cycle also affects the manner in which a defective pixel contributes to the spurious signal. For instance, in the continuous vertical transfer mode of operation used in the EOSP system, the amount of time which a packet of signal charge spends in a particular pixel site is dependent on the clock frequency of the image register gates, and the quantity of charge injection by a defective pixel is proportional to the time of occupancy. Since every charge packet transferred through a defective pixel will pick up the same amount of spurious charge, one defect site will affect many charge packets and in a television display will appear in the image as a high current vertical line. However, in the signal processor application the useful output signal from a vertical column consists of only the one packet containing a particular charge summation. It has received the one slug of spurious charge which was introduced during the transfer through the defective pixel, so this fixed amount of charge, if it is less than a full well, could be subtracted from the summations made in this column register.

The experience with analyzing blemishes has helped establish improved processing criteria for devices and, following the evaluation of devices from each run, will assist us in making meaningful changes in the subsequent wafer runs.

The types of image defects which have been seen most frequently in the TV display of the signal from gated output devices examined thus far are white vertical lines (high current column registers), black vertical lines, and black horizontal lines. Inter-electrode leakage in the gated-output stage has prevented proper operation of the dump cycle in some samples and is probably responsible in other samples for the inability to transfer the image register charge into the output register.

2.4 OPERATION OF A BURIED CHANNEL CCD IMAGER

2.4.1 General Characteristics of Buried Channel CCD Operation

The characteristics of a buried channel CCD are determined by four design parameters; the p-doping density of the silicon substrate, the n-doping density of the ion implanted layer (for an electron conducting device), the density profile of the implanted layer at the end of processing, and the thickness of the gate oxide layer. When the source/drain diffusions are biased to remove all free conduction electrons from the implanted region a positive space charge region is formed having a parabolic potential such as is shown in Fig. 2-7. The potential difference between the conduction bands of the substrate and the well minimum is called V_{mb} and, as shown in Fig. 2-8, its value increases with increasing gate voltage. The potential difference between the conduction bands of the $Si\text{-}SiO_2$ interface and the well minimum is called V_{mo}. Its value decreases as the gate potential increases. Note that both V_{mb} and V_{mo} vary with the amount of charge in the well. To prevent interaction between the charge in the well and the surface states a minimum value for $V_{mo} \approx 0.25V$ is required. Thus, under certain conditions of gate voltage and well filling when $V_{mo} \approx 0$, the device can shift from the buried channel to the surface channel operating mode as evidenced by a large increase in transfer loss.

Also shown in Fig. 2-8 is the constant value for both V_{mb} and V_{mo} which occurs at gate voltages less than a particular negative value. This occurs when the valence band of the interface and the substrate reach the same value and the interface is "pinned" by the positive charge from the p+ channel stops. Typical empty well values of V_{mb} vs V_g for the test transistors of chips on the three wafers examined thus far are shown in Fig. 2-9. The difference between the storage gate (1st level poly) and the transfer gate

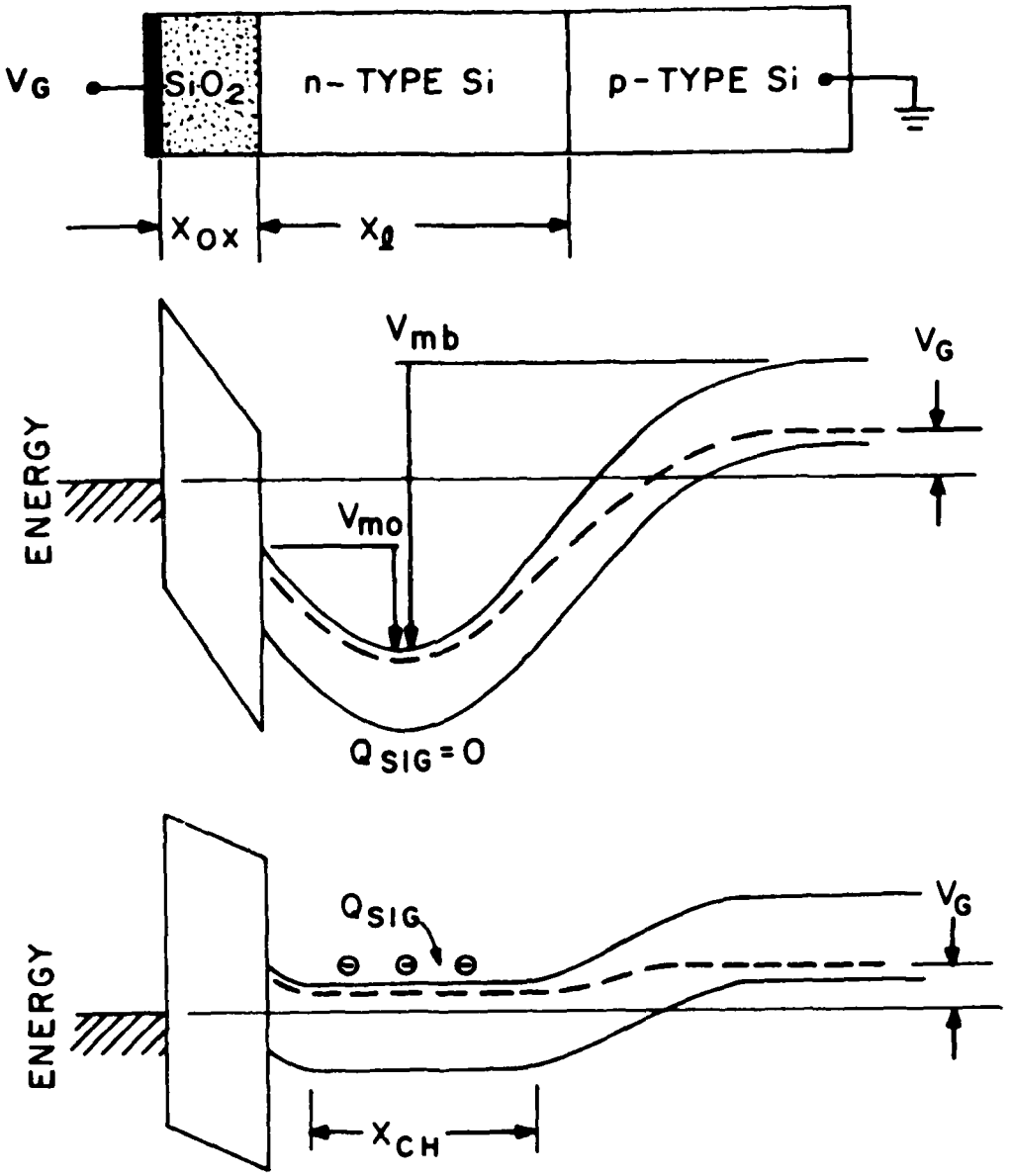

Figure 2-7. Energy profile of the buried channel well.

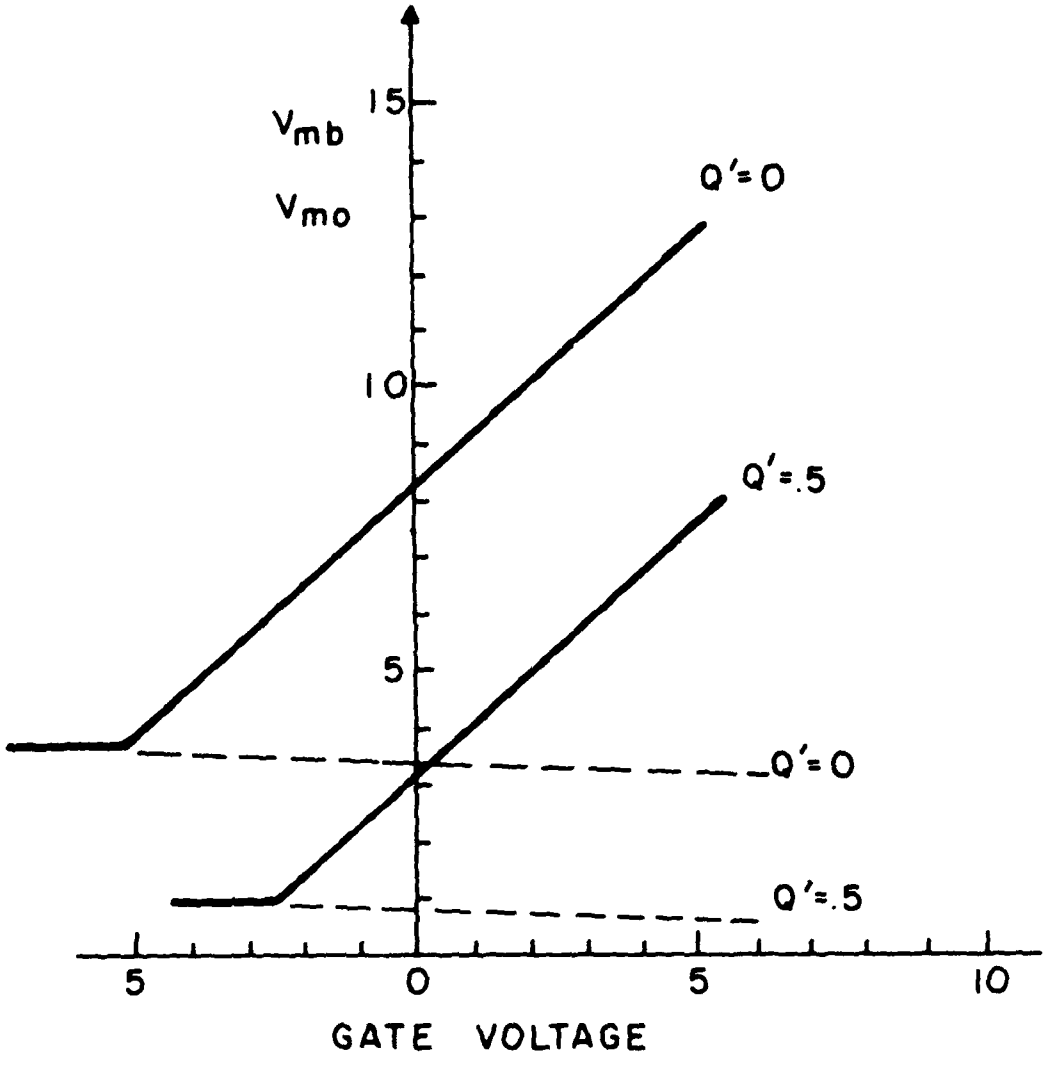

Figure 2-8. V_{mb} (solid line) and V_{mo} (dotted line) as a function of gate voltage.

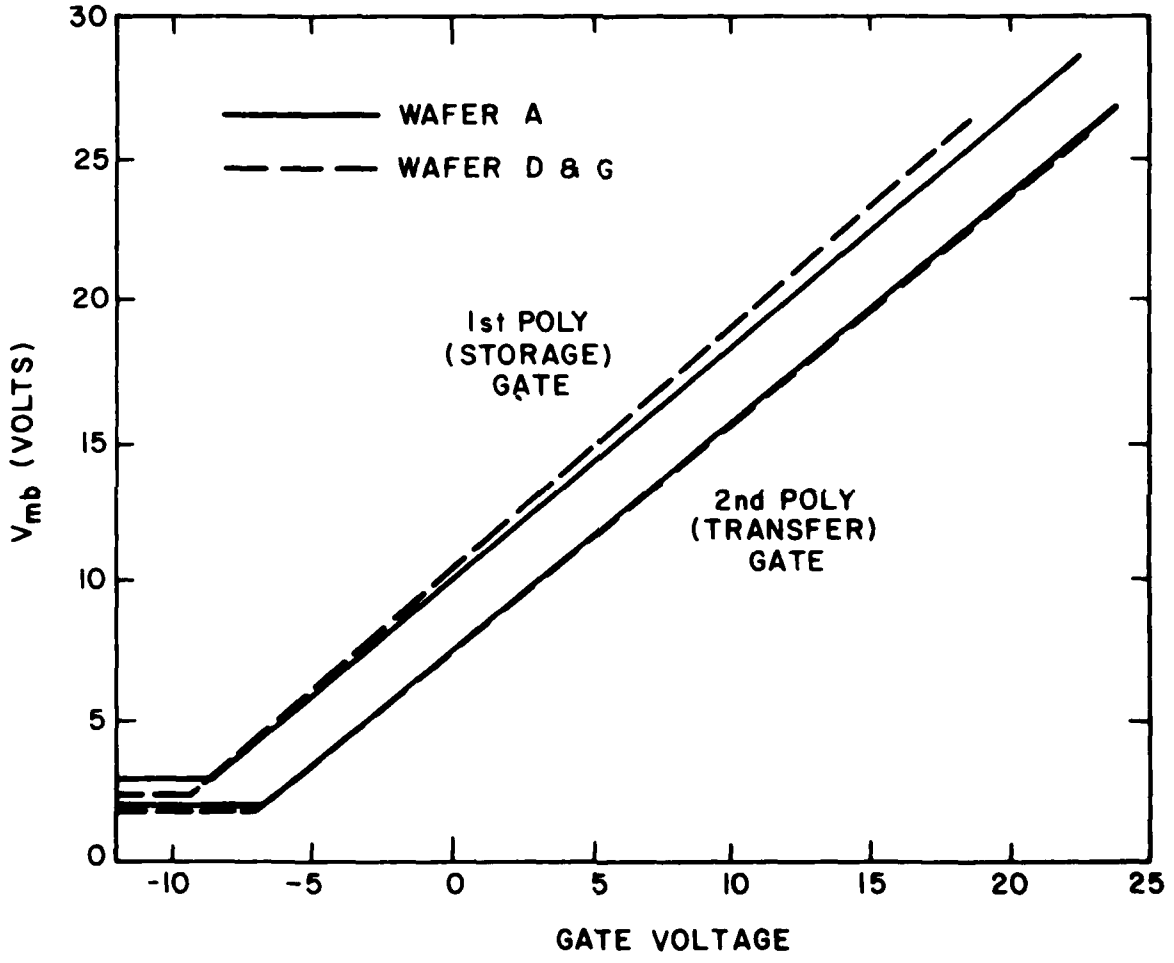

Figure 2-9. Measured V_{mb} vs V_G ($Q' = 0$).

(2nd level poly) is probably an indication of a difference in gate oxide thickness.

The desired channel potential profile under the four gates of one stage is shown in Fig. 2-10. If the $\phi 1$ transfer gate voltage V_T OFF is set at or close to the pin voltage of the empty well and if a $\phi 2$ storage gate voltage V_s ON voltage is selected, then the difference in V_{mb} represented by these gate voltages must be subdivided into $\Delta V_{mb} + 0.5 + \Delta V_{mb}$. The half-volt difference between the $\phi 1$ storage gate V_s OFF and $\phi 2$ transfer gate V_T ON is required to assure complete charge transfer in the intended direction.

The maximum charge per unit area (Q' = 1) for the well formed under a positively biased gate is determined by the implant dose of the n-channel. Fig. 2-11 shows that the full well charge capacity Q' increases as V_s ON increases. Also shown on this plot is a demarcation between the domains of buried channel and surface channel operation. At values of V_g for which Q' is below this demarcation line the CCD will remain in buried channel operation as the amount of charge in the well is increased until the full well level is reached. A further increase in charge will cause the over-filled well to "bloom" by spilling charge into adjacent pixels. At the higher values of V_g for which Q' falls in the surface channel domain (that is above the demarcation line) one observes an abrupt increase in the charge transfer loss as the amount of charge in the well is gradually increased. This marks the transition from buried to surface channel operation. Since there is a value for V_g which provides the maximum Q' for buried channel operation, the correct V_s ON value can be read from this plot. Peak buried channel values for Q' in the order of 0.5 to 0.6 are typical of a good choice for the four basic design parameters.

2.4.2 Experimental Performance of the Gated Output Devices

The 30 Ωcm ($N_p = 4 \times 10^{14}$ dopant atoms/cm^3) p-type wafer on which the devices have been constructed is given an implant with boron atoms to a density in the order of $N_n = 2.7 \times 10^{16}$ atoms/cm^3 and a layer thickness of 0.5 μm after processing has been completed. Fig. 2-12 shows the calculated full well charge density Q as a function of gate voltage V_g. The measured value of the maximum buried channel full well charge in the image area is between 8

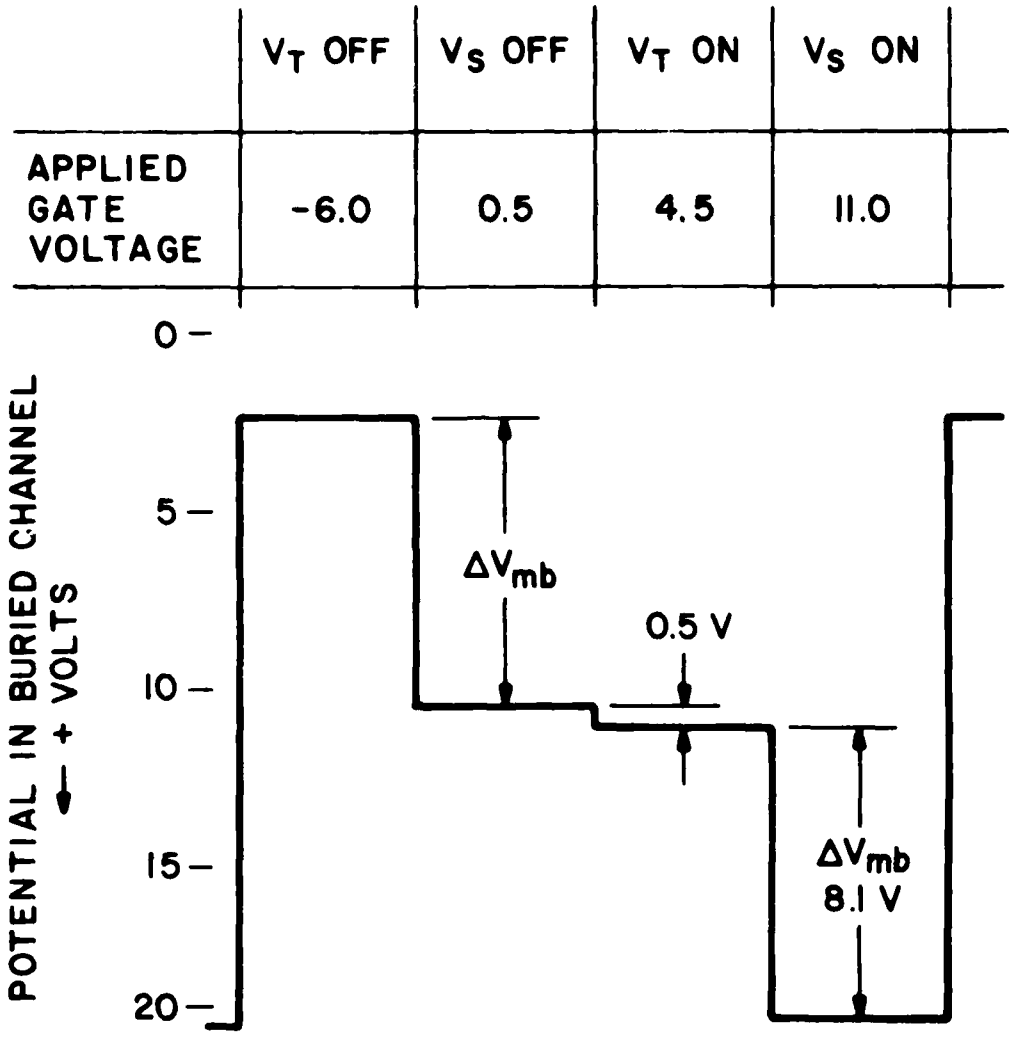

Figure 2-10. Energy levels under the gates for operation of a two-level two-phase CCD ($Q' = 0$).

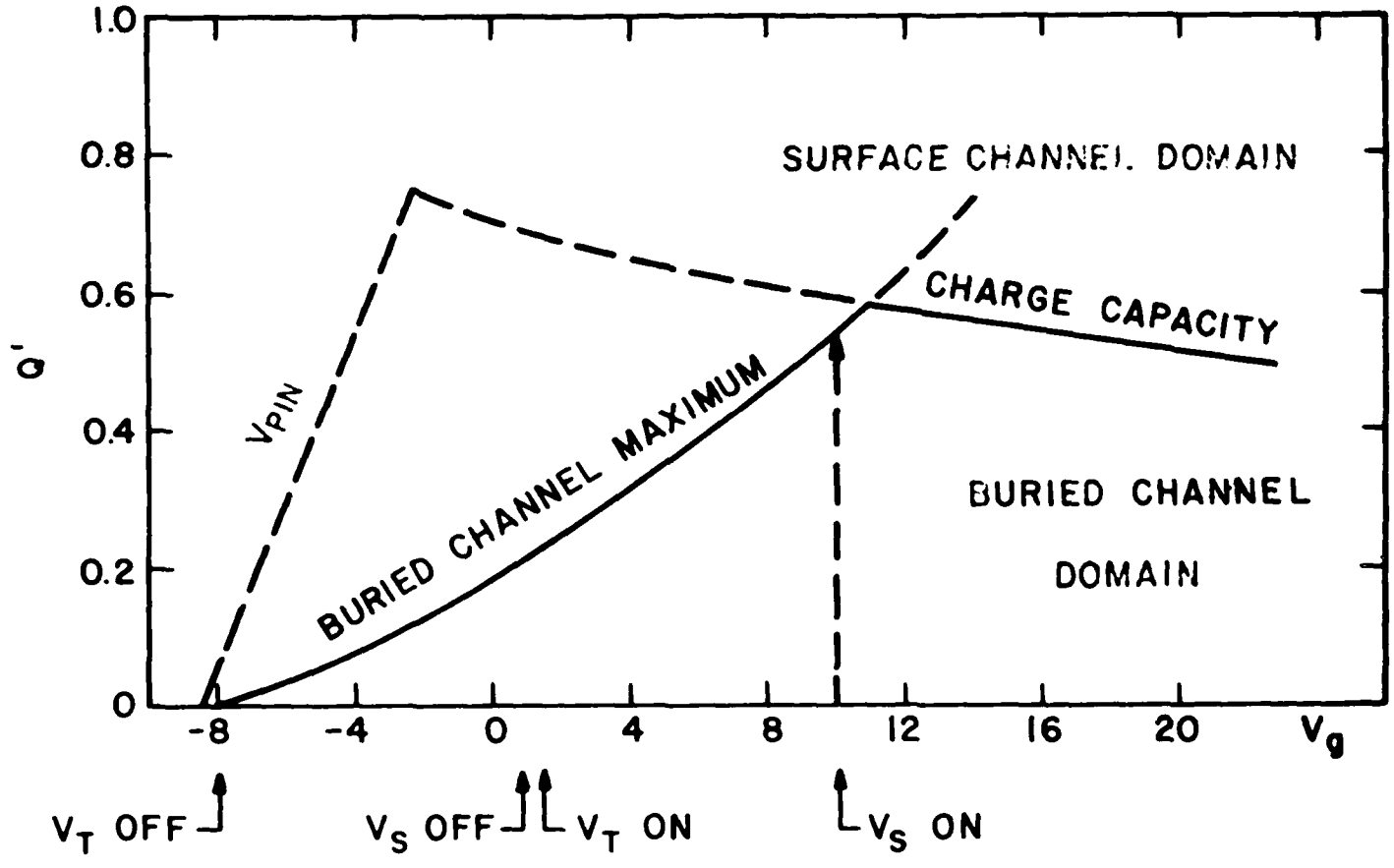

Figure 2-11. Full well buried channel Q' vs V_g for Gated Output CCD.

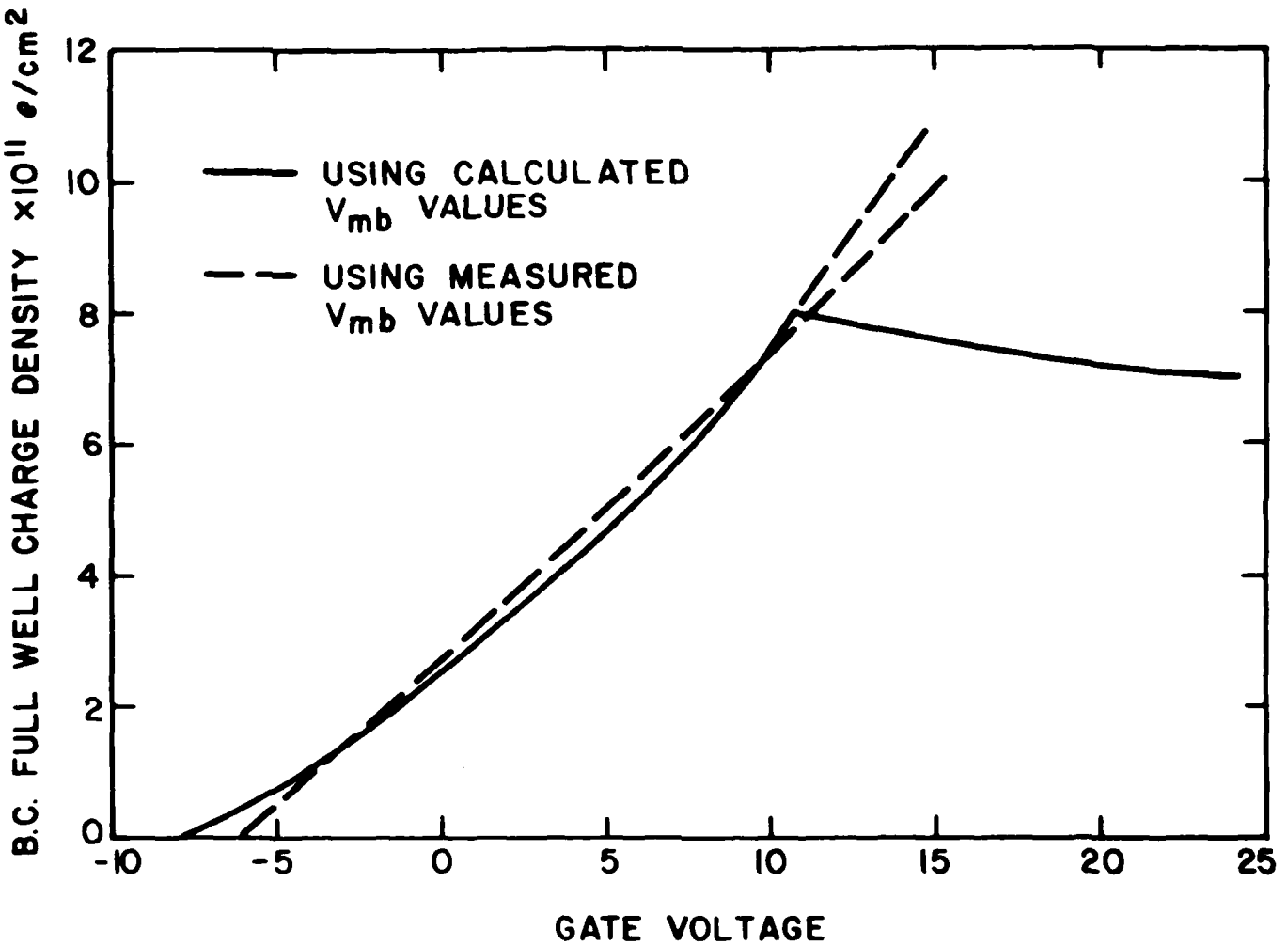

Figure 2-12. Calculated full well buried channel well capacity vs V_g for first run CCD devices.

and $9x10^6$ charges/pixel. This is essentially the same as that predicted by the calculated performance shown in this figure. Somewhat higher V_{ON} values have been required for the storage gates of the image area than for the output register gates.

These data represent the early results from the devices. More extensive investigation of various operating variables which could affect the linearity of the transfer characteristics will be carried out in the future.

Fig. 2-13 shows the photosensitivity of the image area in terms of quantum conversion efficiency vs. illumination wavelength for a run 1 device.

2.5 CONCLUSION

The gated output CCD Imager with its gate-controlled output stage has demonstrated that it meets the design objectives for the Electro-Optical Signal Processor application. Although only a limited number of devices from the first fabrication have been examined, the performance results have been encouraging and all components of the total structure have been observed to function as intended. The buried channel 50x50 μm pixels of the image area have a full well charge capacity in the order of $8x10^{11}$ e/cm^2 and a dynamic range in excess of 500 to 1 without use of the dummy output register.

The observed photosensitivity of the image is uniform, with the most prevalent cosmetic defects being white vertical lines (high current columns), black vertical lines, and black horizontal lines.

Compared with the SID type imager, the gated output CCD with its two-phase overlapping gate structure is very tolerant and forgiving of the shape and the overlap of the applied clock pulses. In our investigation of the maximum usable clock frequency for the image area gates, the vertical resolution was not degraded despite the considerable distortion of the clock pulses as the clock frequency increased. Only when a frequency in the order of 5 MHz was reached did the increased transfer loss resulting from a reduced pulse amplitude and major departures from square wave pulse shape cause the resolution to become degraded

The optical memory mask, Test Mask #1, which was formed on the surface of the image area of the devices of one wafer has been given only a limited evaluation at RCA Labs. Two chips from this wafer were delivered to NOSC for initial evaluation in the signal processor application. The small apertures

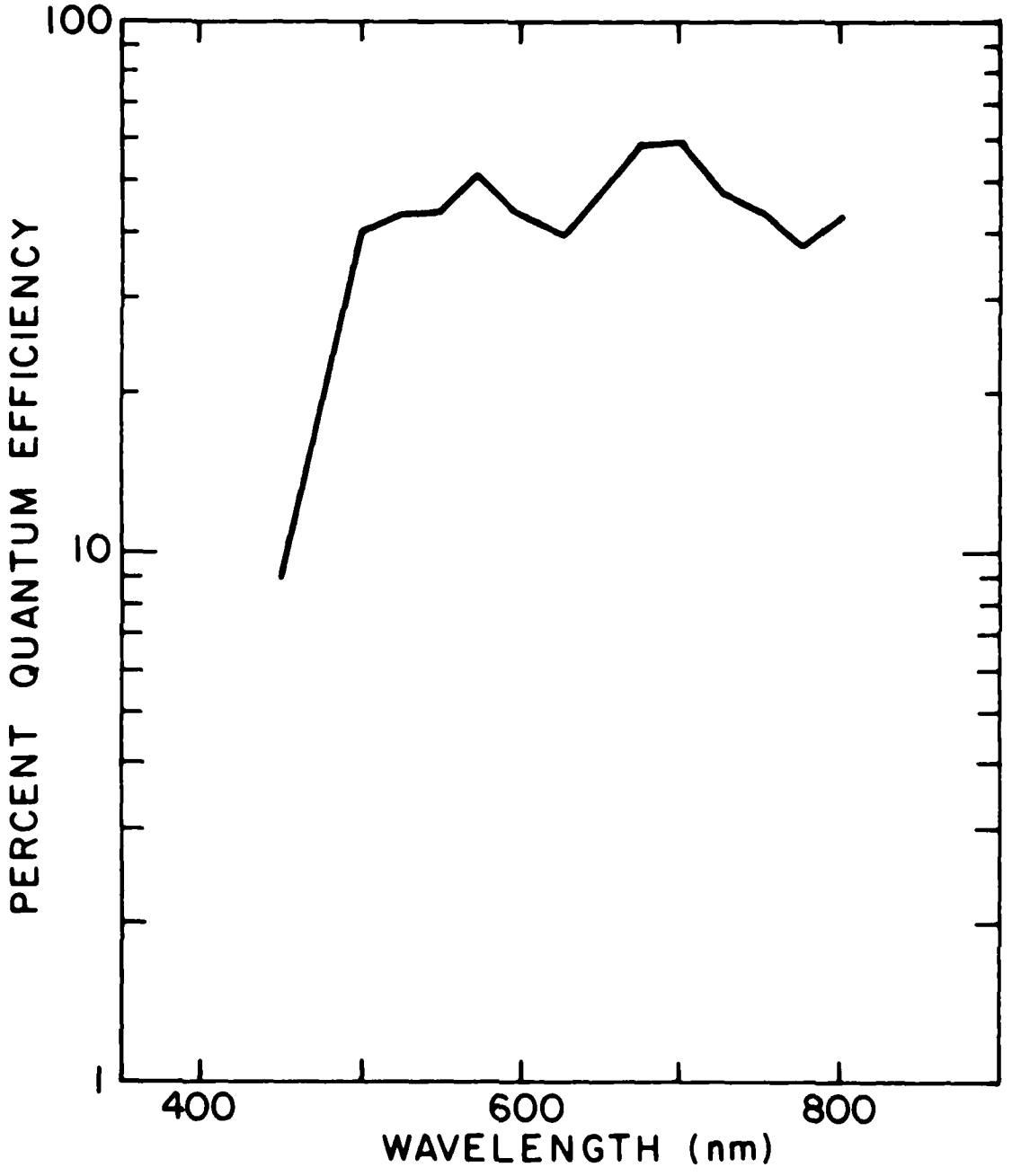

Figure 2-13. Quantum conversion efficiency vs illumination wavelength of the Gated Output CCD.

of the four lines having aperture area sequences were poorly defined in this first mask fabrication on the two-level structure. Despite this, the transfer function of aperture area vs. signal was linear except for the apertures 5 μm or smaller in width (height 8 μm). There is insufficient data to determine the minimum Δ area increment.

With the follow-on program already in progress* a more complete evaluation of performance will be carried out at RCA Labs with the examination of the remaining devices from Run 1 and subsequent fabrications. These test results will be compared with performance data acquired by NOSC. A major effort will be applied to the particular problem of improving the dimensional accuracy of the apertures formed in the integral optical memory pattern covering the CCDs in order that improved samples can be supplied to NOSC for their systems operation and evaluation.

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*N66001-80-R-0223
Masked Gated-Output CCD - Phase I

3.0 MASK PREPARATION

3.1 TEST MASK

As stated in the RCA report, the gated output CCD has been fabricated with an integral chromium metal mask. There have been two types of masks used to date. (Also, some devices were fabricated without masks).

The first mask was the test pattern described in section 2.2.3 and is shown in Fig. 3-1. The purpose of this mask is to test the characteristics of the CCD as an imager and determine parameters such as:

a. uniformity of response over the array

b. cross-talk between the rows and columns

c. linearity of the masking process, i.e., how well does the value of an aperture (or the number of electrons read out from a given pixel) correspond to the design value. The results of the tests using this mask have been very informative and are discussed in section 6.

3.2 THE DFT MASK

The second mask is the DFT mask. This mask enables the CCD to be used as a multichannel correlator and perform the Discrete Fourier Transform on the input signal. A representation of the mask, showing the pixel aperture values is shown in Fig. 3-2.

The mask consists of an array of apertures arranged as a matrix of 128 rows and 128 columns. A column corresponds to a particular frequency of interest in multiples from 1 to 64. The cosine of frequency 1 is on the left side of the mask, in column 1. The sine of frequency 1 is in column 65. On the actual device, the output register is at the bottom of the figure, with the output on the left hand side.

3.3 APERTURE SIZES

The size of the aperture down any cosine column is defined by the equation:

$$T = 1/2 + 1/2 \cos (2 F/128)$$

where T = the transmission of the aperture;

F is the frequency (1-64).

The transmission varies from 0 to 1.0.

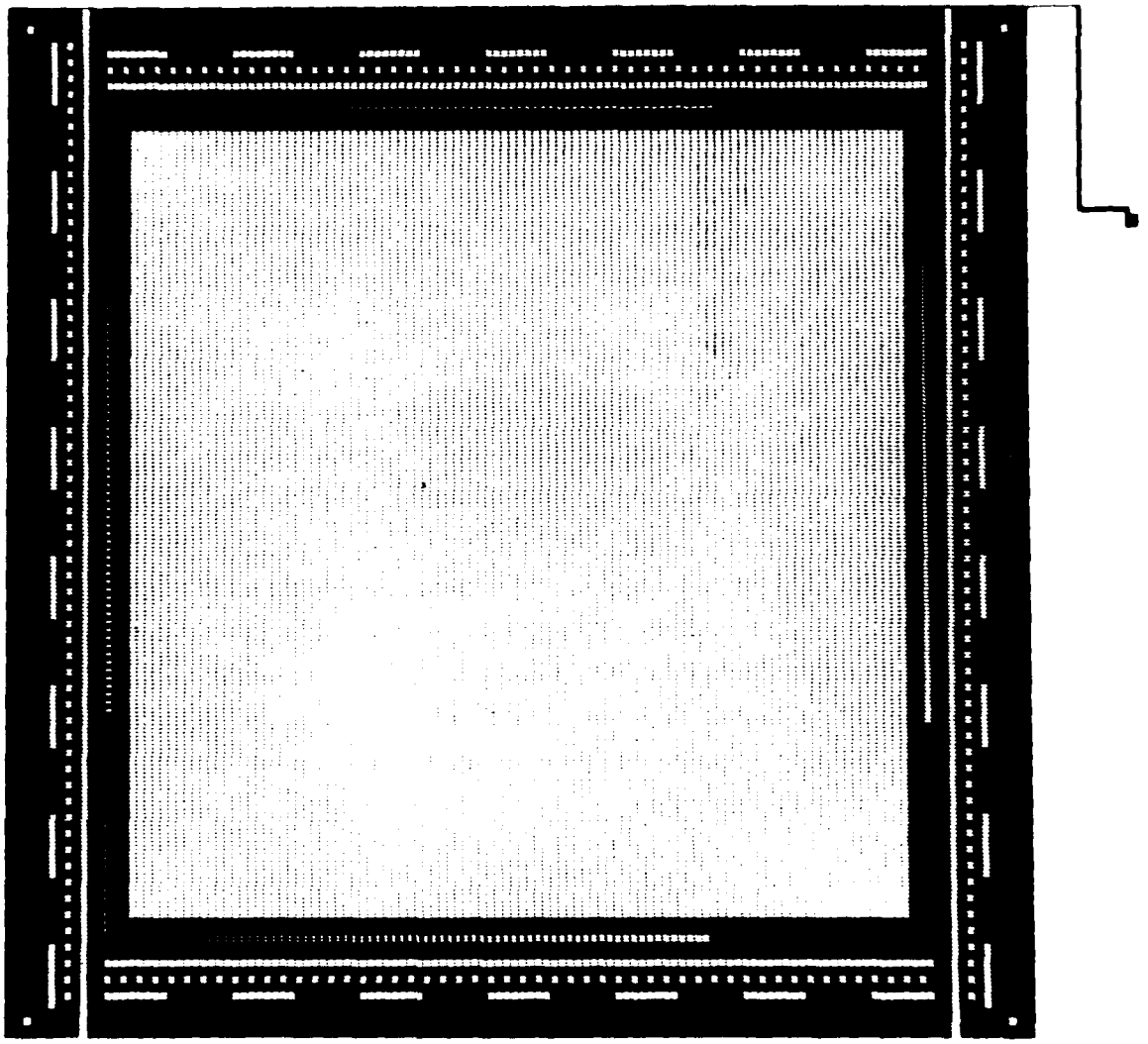
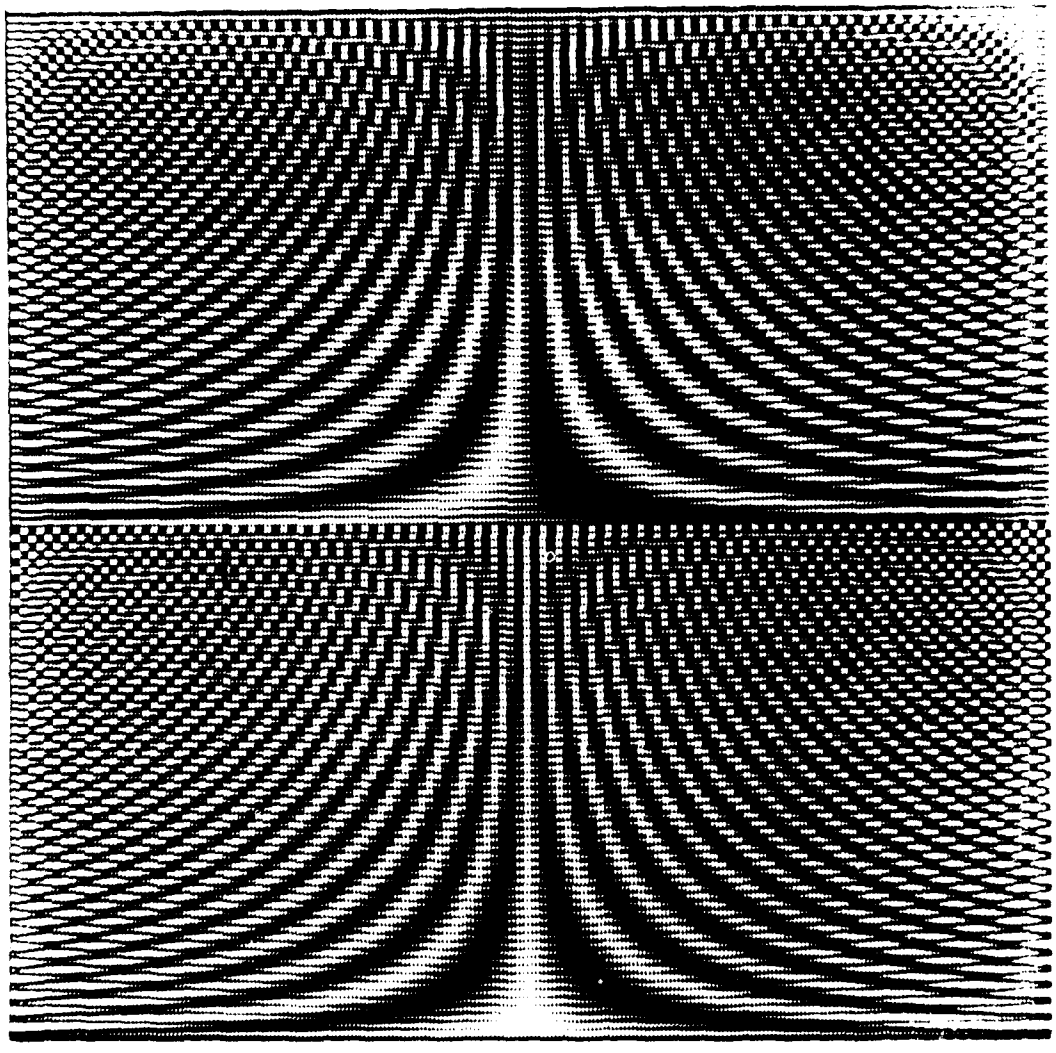


Figure 3-1. The test mask.



Since there are two areas in each pixel, the transmission value must be converted to two rectangular openings in a given pixel.

There are many factors which could influence the accuracy of the apertures in the mask. These have to do with the many steps required in the fabrication of the device. For instance, the etching of the aperture into the chrome is not controlled to better than ±5%. Exposure of the photoresist can cause variations in aperture size. Bounding of the corners in small apertures (2-3 microns on a side) will have an effect on small apertures relative to large ones. Long, thin apertures can have larger percent variation than square ones for the same processing variations. Also, there can be some variation in the thickness, and hence transmissivity, of the polysilicon layer under the aperture.

3.4 THE MASK PRODUCTION PROCESS

This paper has discussed two of the numerous transforms which the EOP can perform and given examples of typical masks in the illustrations. These illustrations are reproductions of simple plots made by our minicomputer plotter using a felt tipped pen.

The mask used in our current EOP is formed by etching holes in a chrome layer on the silicon wafer using standard photolithographic techniques. How then does one proceed from a concept of a mask to something which can be used by the people who make chips? There are five basic steps:

1. Define an equation for pixel transmittance as a function of the pixel row and column position.

2. Define a mapping from transmittance of a pixel to dimensions for the opening(s) in the opaque mask layer.

3. Insert these two relations into a skeleton program which writes a computer tape in industry standard format.

4. Read the tape into a pattern generator machine which exposes the pattern onto a chrome on glass reticle.

5. This reticle is then used in a photolithographic process to etch openings into the chrome layer on the silicon wafer.

3.5 THE TRANSMITTANCE FUNCTION

The choice of the transform or correlation to be performed defines the type of function to be used. For instance, the Fourier transform requires sine and cosine functions. Transmittance, however, does not permit negative values. A choice must be made between the use of a bias

$$T = 1/2 + 1/2 \sin(\theta)$$

or the use of additional hardware to combine a two column output such as would result from

$$T_{\text{positive column}} = \begin{cases} \sin\theta; & \text{for } \sin\theta \text{ positive} \\ 0 & \text{; otherwise} \end{cases}$$

$$T_{\text{negative column}} = \begin{cases} -\sin\theta; & \text{for } \sin\theta \text{ negative} \\ 0 & \text{; otherwise} \end{cases}$$

Continuing with our Fourier Transform mask, one must now define a relation between θ and the row and column number. If frequency changes with the column number, and the rows represent time, we need a function such as:

$$\theta = \frac{2\pi RC}{N_r}$$

where N_r = number of rows in the mask

R = Row number from 0 to $N_r - 1$

C = Column number from 0 to $N_c/2 - 1$

Notice that our top and bottom rows are different. To be truly periodic, the values for $\theta = 0$ and $\theta = 2\pi$ must not both appear in a sampled cycle of the sine wave. Also note that we chose a phase of zero where $R = 0$. This could also have been chosen to appear in the middle of the mask if we wish to work with negative time. Turning to the frequency variable, the sample equation for T above includes a frequency = 0 term with all cells in the first column closed. The value of C ranges only to $N_c/2 - 1$ to cover equally spaced frequencies up to, but not including, the Nyquist rate. Other design choices would lead to a different transmittance function depending on the desired application. If the application is spectral analysis, the sine term in the transmittance function will need to be multiplied by a window function such as a form of Kaiser-Bessel function which is normalized to range between 0 and 1.

3.6 THE TRANSMITTANCE TO PIXEL OPENING RELATION

What transmittance causes what size hole to be opened over each pixel? This obviously depends on the CCD geometry. If the mask is likely to be misaligned over the CCD, one might trade off reduced dynamic range against alignment tolerances by leaving an opaque guard area around the openings by limiting T = 1 openings to less than the photosensitive area of a pixel.

Generators such as the electromask machine cannot produce arbitrarily small openings. Usually, this is substantially larger than the quantization and usable resolution available on the machine. Photographic processes often cause edge migration and corner rounding dependent on exposure and the developing techniques used. To the extent that these are predictable, masks can be designed which compensate for such errors.

3.7 CREATION OF A PATTERN GENERATOR TAPE

NOSC has developed a general purpose skeleton FORTRAN program for creating pattern generator input tapes. First, the transmittance function which returns transmittance as a function of row and column number is merged into the skeleton. This function varies with the application, but not with the type of CCD to be used. Next, a subroutine is added which inputs transmittance values and generates calls routines which write rectangle height, width and position commands on the tape.

Fortunately, there are standards for these pattern generator tapes. The format used at NOSC was designed for Electromask Corp. machines, but competitive machines such as those from D. W. Mann can accommodate them. Recently, the conversion from optical to E-beam went smoothly since conversion to raster information could be handled by a utility program already developed at RCA. Although standard formats exist, partial implementations can cause problems. Electromask Corp. allows ASCII or EBCDIC tape codes and records up to 800 bytes long. The "compatible" implementation supported only EBCDIC and records exactly 800 bytes long. Another confusion factor arises when the reticle is used. The pattern generator exposes it emulsion side up, yet the silicon wafer is exposed with the emulsion side down. To reduce the possibility of error each reticle is marked by the skeleton program with the word "emulsion" outside of the useful field on the ouput corner of the chip. If the word can be read, the emulsion side is up.

Since each mask costs over a thousand dollars, such mistakes are costly. An interactive program was written to perform extensive syntax checking and produce check plots on paper from the computer tape.

3.8 CREATING THE CHROME ON GLASS MASTER

When the pattern tape arrives at the semiconductor manufacturer it is read into an Applicon computer aided design (CAD) facility where openings are added for the lead bonding pads.

At this point one may wonder why the CAD facility was not used to generate the entire pattern. Typical patterns encountered in integrated circuit designs are entered by digitization of drawings with some help from pattern repetition routines. Unfortunately, these CAD systems have no facility for mathematical languages such as FORTRAN. Optical pattern generators such as the Electromask and D. W. Mann machines consist of individually programmable X and Y stages which position an emulsion coated glass plate. A flash lamp and lens is mounted above the X-Y stage. A rectangular aperture programmable in width and height is imaged onto the emulsion. The X, Y, height and width servo systems are each equipped with laser interferometer position sensors.

Electron beam pattern generators use a raster scan and fixed size beam to scan the entire image. Utility programs exist to convert electromask format tapes to raster information suitable for turning on and off the electron beam at the proper times.

4.0 THE TEST SYSTEM

4.1 TEST SYSTEM - OVERVIEW

In order to evaluate and utilize the capabilities of the Gated Output CCD a complete test system has been designed which will allow precise control and measurement of the EOP characteristics. Previous work was driven by the necessity of building working EOP hardware for a particular system application and was very frustrating since it did not allow careful analysis of the fundamental characteristics of the EOP. With the development of the GO/CCD and use of a comprehensive test system, the capabilities and limitations of the EOP can be explored.

The test system consists of a HP-1000 computer system and specially designed electronics to control the operation and measurement of the EOP. A block diagram of the system is shown in Figure 4-1. The operator controls the system through the CRT/keyboard connected to the HP-1000 system. Three channels of the HP-1000 are used. The first channel is used to load a buffer

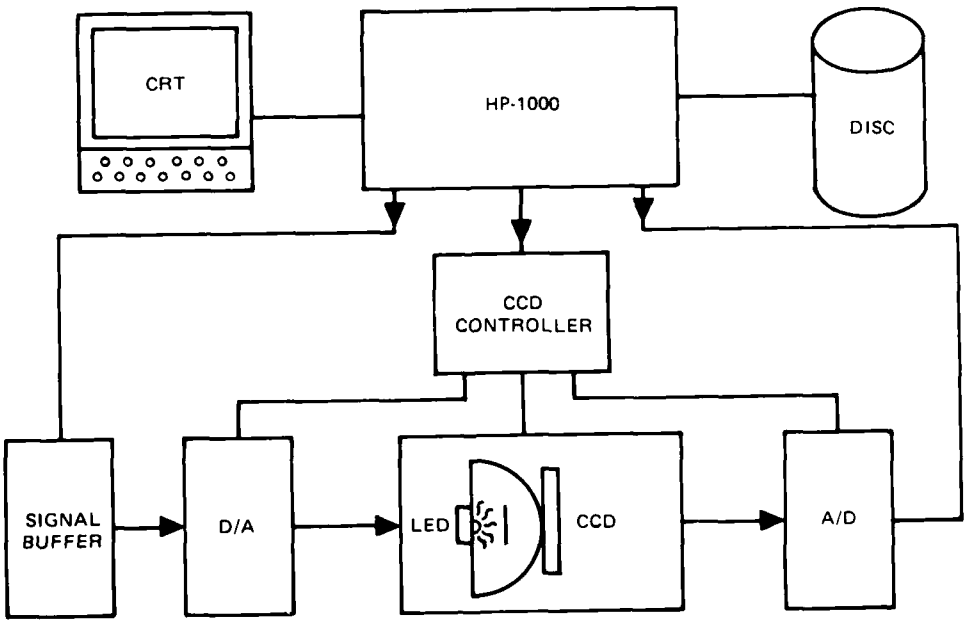


Figure 4-1. CCD test system.

which drives a digital-to-analog converter (D/A). This allows the operator to generate controlled input signals for the EOP. A second channel passes the control information to the controller. The controller is basically a RAM which is sequenced and generates the timing of various control and clock lines required by the EOP. The controller is required since the HP-system will not generate signals at the 10 MHz rate required to control the EOP and associated equipment. The control lines can be changed "instantaneously" by the operator to determine effects of timing changes on the operation of the EOP. The third channel is connected to the analog-to-digital converter (A/D) and buffer which provides digitized values of the output of the CCP for later analysis by the operator.

The HP-1000 System has been essential in this work. It has several CRT/keyboard terminals for program generation, and other useful peripherals such as a hard copy printer and a large disk memory which will be used to store the large programs necessary for CCD testing as well as the data taken from the EOP. This data storage could be several hundred thousand 16 bit words, accumulated from several devices, with different timing and test patterns.

The HP-1000 System supports the FORTRAN-IV language presently. All programs were written in FORTRAN IV. The I/O channels can be run with DMA to achieve approximately 1 Mega word per second rate.

4.2 THE CCD CONTROLLER

The CCD controller accepts 16 bit words from the HP system and stores them in RAM. With appropriate control signals the controller will sequence through RAM, generating the desired control lines for the EOP and other equipment. A block diagram of the CCD Controller is shown in Figure 4-2.

The CCD Controller is loaded by the HP-1000. Six commands determine the controller function. The three most significant bits of the HP 16-bit word determine the command.

The Clear command (Function Code (FC)=1) clears all the registers and initializes the controller.

The Load Control RAM command (FC=2) loads the RAM with the lower eight bits of the 16 bit word. Since the control RAM is 1024 words by 32 bits wide, this command must be used 4096 times to load the RAM completely. Internal counters sequence through the RAM address space.

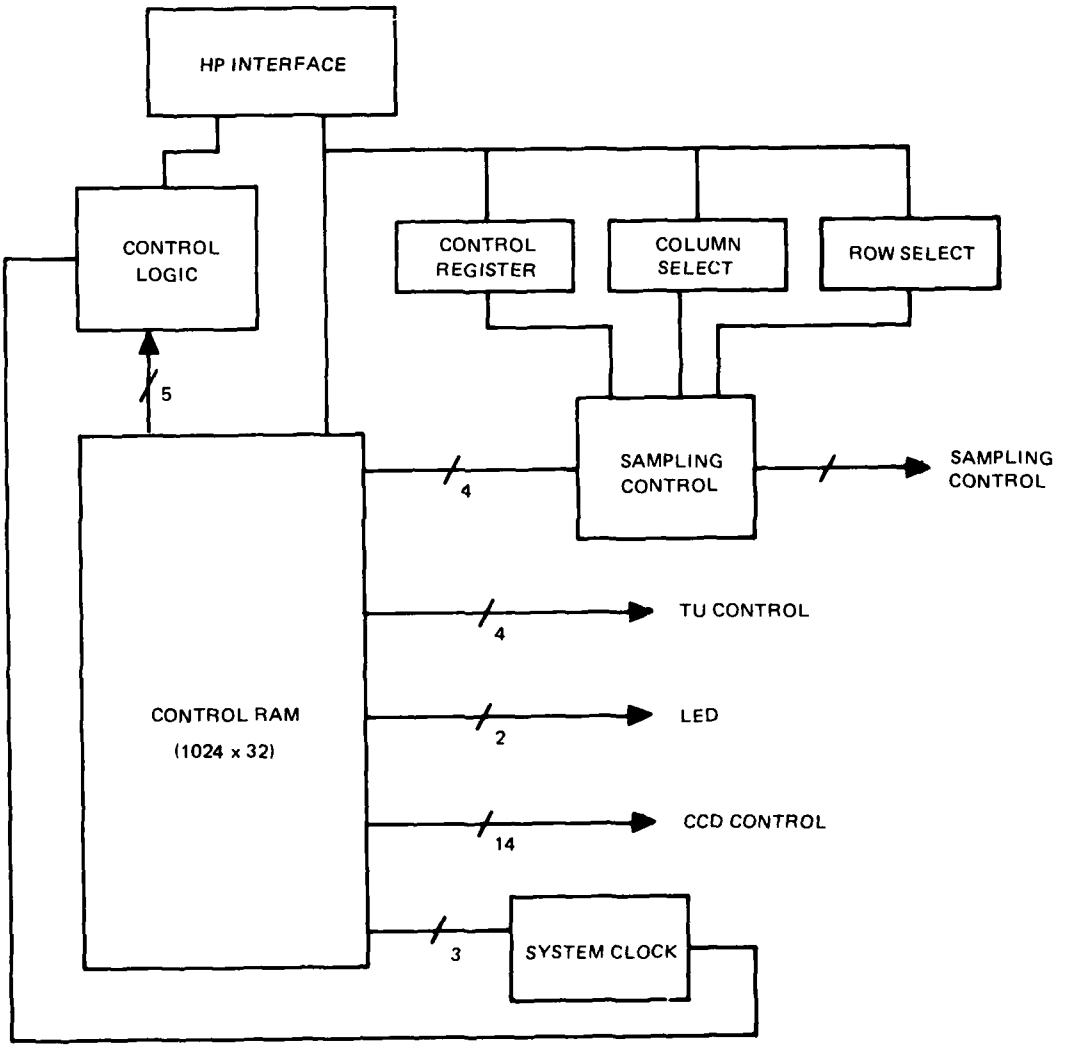


Figure 4-2. Controller block diagram.

The Load Control Register command (FC=3) loads the internal control register. This register controls the operation of the controller while it is sequencing. Bits 0-3 specify the number of rows or columns to be sampled (1-to-16) during the data taking operation. Bits 4 and 5 of the control register select the row or column sampling mode. Bits 6 and 7 determine the manner in which the controller stops itself: 1- no stop, i.e., continuous running; 2- after one row of 128 pixels; 3- after 2048 samples of data; 4- after a complete frame has been sequenced through (128x128 pixels).

The Load Column command (FC=4) command loads the column select register which selects the first column to be sampled.

The Load Row command (FC=5) loads the row select register which selects the first row to be sampled.

The Start command (FC=6) which is used to start the sequencer through the previously selected mode of operation.

The only other inputs to the controller are thru two push buttons on the front panel. One button master clears the controller and the other starts the controller running with the existing control register information.

The RAM contains the information which controls the CCD clocks and other operating characteristics of the system. There are 1024 32 bit words. Each bit is a control line. Fourteen bits control the CCD, i.e., control gate potentials and shift clocks. Four bits control the TV display clocking. Three bits control the clock period, i.e., any of the 1024 control words can be held on for eight binary multiples of 100 nanoseconds, (100, 200, 400, 800 etc.). Four other bits are used to control the sampling of the CCD output. Two control bits determine the clocking of the LED signal. The remaining five bits control internal logic for counting pixels and miscellaneous control functions. A list of the control bits is shown in Table 3-1.

The RAM is loaded from the HP-1000 system. The Control Generation (CG) prgram interacts with the operator to load the appropriate information into the RAM. The operator simply sets a particular bit high when he wants the control line to go high. Similarly for the low state. The CG program has a menu of functions and prompts the operator for response. A timing diagram like output can be obtained on the CRT or in hard copy on the printer. Details of operation of the CG program are explained in the section on software.

TABLE 3-1

Control Bit Names and Numbers

Bit	Name	Bit	Name
1	VBG (DUMP)	17	CK SL A
2	VGDS	18	CK SL B
3	VR2 (RESET)	19	CK SL C
4	VTOT (VT2)	20	LN LD-BAR
5	VTIN (VT1)	21	PXCK-BAR
6	VIN (1-2)	22	FRMCLR-BAR
7	VS (VSRC)	23	RESTLN-BAR
8	VG3 (1-2)	24	CLMCLK-BAR
9	SPARE	25	CONVRT-BAR
10	SMPL HOLD	26	CLR ADCBFR
11	VRT CLK	27	TRIGGER
12	HRZ CLK	28	SMPL PULSE
13	D/A ENBL	29	TVCLK-BAR
14	LED CLK	30	TVLNRS-BAR
15	FLUSH-BAR	31	TVFMRS-BAR
16	VRT FLUSH	32	TVBLANKING

4.3 THE ANALOG TO DIGITAL (A/D) MODULE

The Analog-to-Digital (A/D) Converter module samples the output of the CCD at a time determined by the appropriate control line. The analog value is converted into an 8 bit digital value. The A/D module has a 2048 word (by 8 bit) buffer to allow storage of 2048 samples.

It was intended to use a Biomation data sampler but peculiarities of the operation of the Biomation made the control and data gathering too complex and cumbersome. We finally designed a simple A/D module using the TRW flash converter and a few RAM chips with a simple interface to the HP-1000. This unit has worked very well.

The operation is very simple. The controller initializes the unit (sets the RAM address to zero) and then provides convert signals at the appropriate time. The TRW converts the CCD output to the 8 bit digital value which is automatically stored in the RAM. The RAM address is then incremented, so it

will be ready for the next data sample. When sampling is complete the control module notifies the HP-1000 which then reads the 2048 samples from the A/D module and stores them in its memory for later use.

4.4 THE DIGITAL TO ANALOG MODULE

The digital-to-analog (D/A) module generates precise analog wave forms from 10 bit digital words supplied by the HP computer. This is required to evaluate the operation of the EOP when a precisely known signal is used as input. The entire system can be calibrated using this easily controlled accurate signal source. Any desired wave form can be generated in the HP and used to calibrate various sections of the system (i.e., buffer amplifiers, the A/D, etc.). The results can then be analyzed in the HP to check accuracy.

4.5 THE SIGNAL BUFFER

The signal buffer is required to supply a constant flow of signal words to the D/A at up to 4 Megahertz rate. The HP System cannot supply data continuously due to operating system overhead and I/O rate limitations.

The signal buffer is loaded by the HP with the desired digital representation of an analog signal. The controller supplies a clock and an enable to the D/A which in turn requests data words from the signal buffer. There are 2048 16-bit words stored in the signal buffer. A repeat mode is available so that the buffer keeps cycling thru the same 2048 words as long as the D/A requests it.

4.6 THE CCD MODULE

The CCD Module contains the CCD, the CCD output amplifier, the LED light source, and the LED driver. The rear view of the module (without the LED driver) is shown in Figure 4.3. The printed circuit board contains regulators and bias and amplitude control circuitry for the 12 control and clock signals required by the CCD. Many of the circuits are similar so the same circuit is repeated eight times for control lines and twice for the horizontal and vertical clocks.

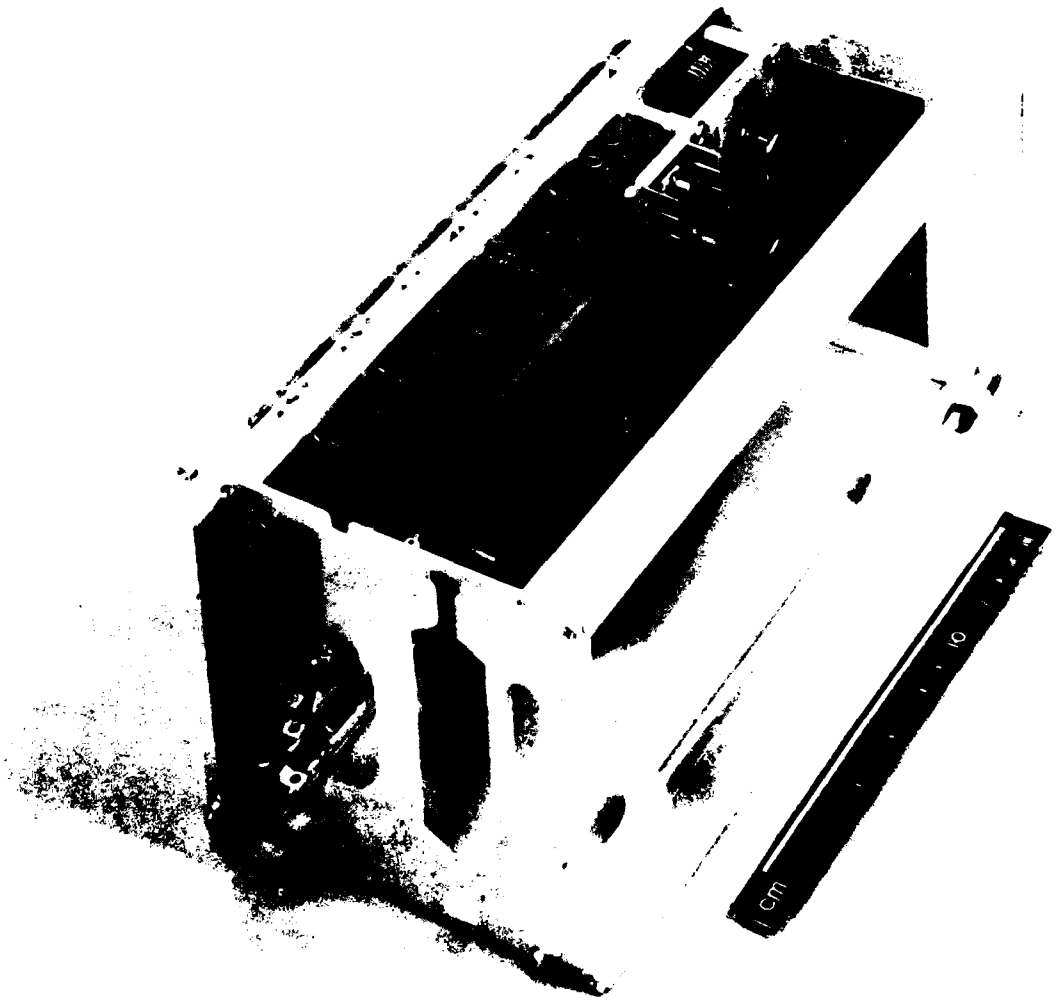


Figure 4.5 The CCD module

CCD Output Amplifier

The CCD output amplifier consists of a differential amplifier, level shifter, sample and hold amplifier, and a buffer driver, Fig. 4-4. There are two output signals from the CCD chip: one is obtained from the horizontal output register which contains both the desired signal and noise due to pickup of the clocking waveforms; the other signal is obtained from a "dummy" register which contains only the noise. These two signals are applied differentially to an amplifier which attempts to cancel signals common to both inputs, i.e. noise, while amplifying only the signal components.

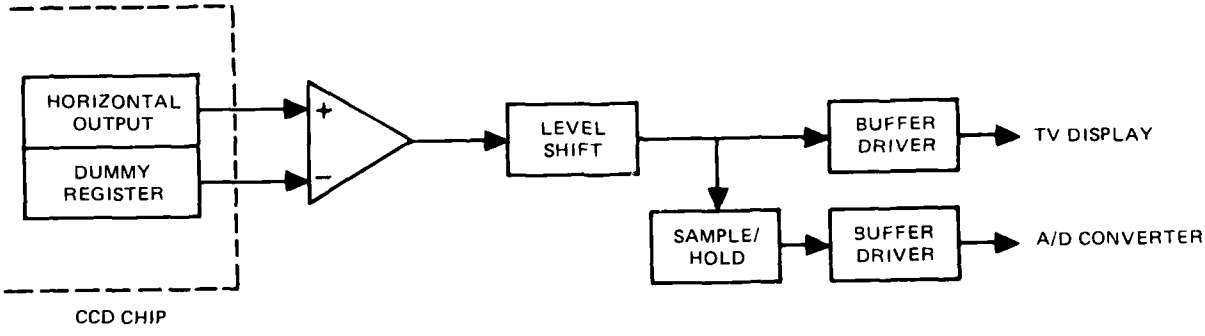


Figure 4-4. CCD Output amplifier block diagram.

The differential amplifier is a wideband high gain device without feedback and has a high output DC level. Hence, a level shifter is used to reduce the output to a level compatible with the TV monitor and A/D converter. The buffer provides the driving capability necessary for 50 ohm coax.

The sample and hold amplifier provides a cleaner signal than is available from the differential amplifier by eliminating the residual clock noise that the differential amplifier cannot remove.

The CCD Module also contains the light source for the EOP. The source is composed of an infrared LED mounted on the flat side of a hemisphere about 3 inches in diameter. The flat surface of the hemisphere is a mirrored surface while the spherical surface is coated with Eastman White, which has a low infrared absorption and uniform scattering characteristics. The goal is to achieve a very uniform illumination over the CCD array so that the input

signal is the same intensity at every point on the mask. The CCD is placed in front of a small (1/2 inch) hole in the sphere directly opposite to the LED. There is a baffle which stops direct illumination of the CCD array by the LED. An exploded view of the LED cavity is shown in Figure 4-5.

The LED driver, which is shown in Figure 4-6, is adjacent to the flat side of the hemisphere.

The LED driver provides a controlled current to the LED in direct proportion to the applied input voltage at speeds up to 30 mHz. A high degree of linearity (<1%) is necessary to ensure that distortion and intermodulation products do not interfere with the desired signal components. Although only 2% non-linearity was achieved, methods for achieving less than 1% non-linearity are being investigated.

The optical power generated by an LED is very nearly a linear function of the forward bias current. In order to realize this linear intensity relation, one of the functions of the driver circuit is to drive the LED from a current source. Hence, it is implemented as a voltage to current converter.

Light is a positive only quantity. In order to produce linear amplitude optical intensity modulation, a bias current is added to the signal current through the LED. This is analogous to the biasing necessary for a Class A amplifier.

During normal operation of the driver, switch S_1 is normally closed and switch S_2 is normally open. These switches are used to observe the effects on the CCD output with and without additional charge generation in the CCD during charge transfer between rows. To prevent charge generation during the charge transfer, switch S_1 is opened, and switch S_2 is closed during this time period, thus turning off the LED.

Amplifier A is a high frequency device operated in a transconductance mode with g_m = 10V/A. The transistor is added to provide the additional current necessary to drive the LED. Note that both the transistor and the LED are within the op-amp feedback loop. Hence, the voltage offsets and their drifts are divided by the amplifier loop gain and are no longer a source for error.

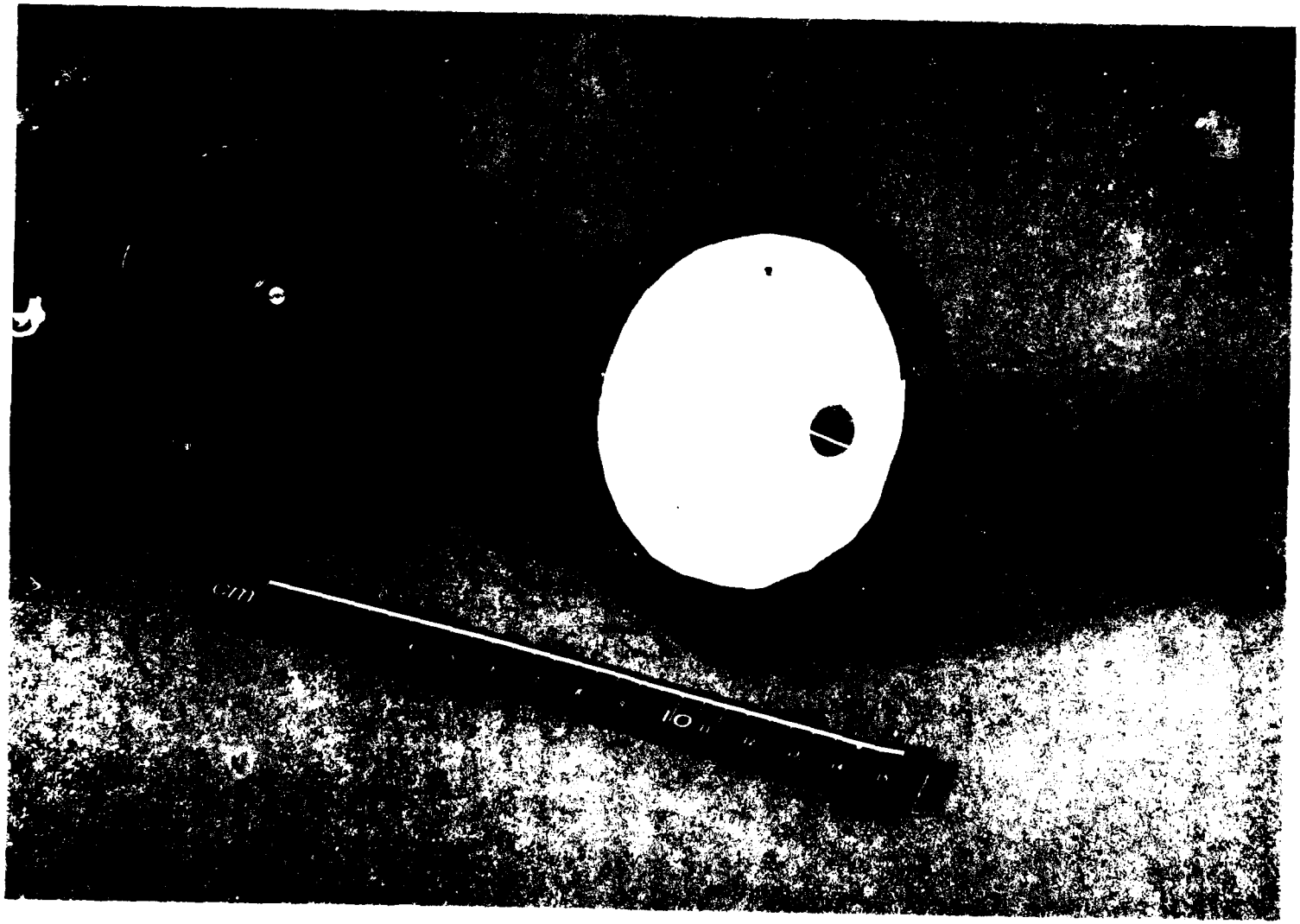


Figure 4-5 LED cavity

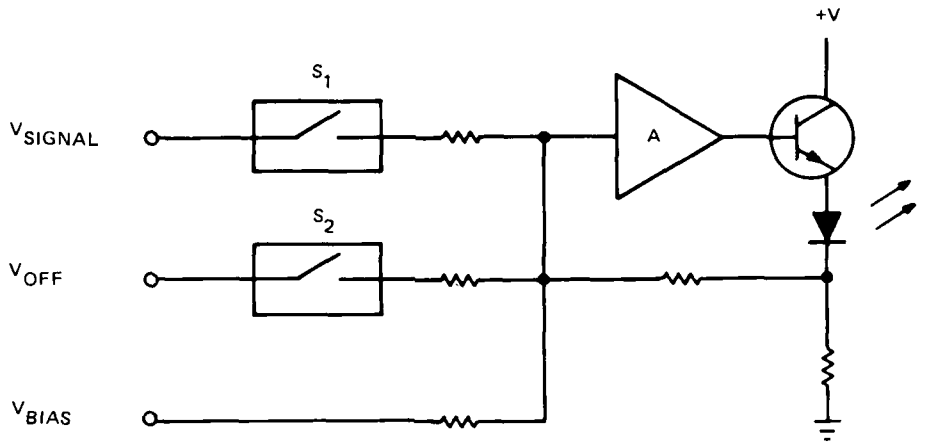


Figure 4-6. Simplified schematic of LED driver.

5.0 TEST RESULTS

5.1 As described earlier the Test Pattern Mask was designed for use as an aid in characterizing the CCD. Parameters of primary interest are: (1) the uniformity of response over the array, (2) cross talk between columns, (3) system precision, and (4) linearity of response. Other parameters which may affect operation are shift frequency, system noise (due to clocks), uniformity of illumination, etc.

5.2 The series of plots presented here represent the best data obtained from devices thus far. There is a broad variation from device to device. The curves will also change with adjustments to the various clocks and bias voltages. The data shown were taken using the TV mode, in which the light source is pulsed on for a short period, then the entire array is read out - similar to an imager.

5.3 The twelve plots, Figure 5-1 thru 5-12, show the amplitude of the signal generated in the 3rd through 15th columns. This signal is proportional to the electrons generated by the openings in the mask as described in section 2.

To start, with column 3, Figure 5-1, note that the individual full open pixels (row 3 and 126) are easily seen. Also note that they have amplitudes of about 100. The middle portion of this column is relatively flat, i.e., average amplitude = 5.5, PK-PK = 13. This flatness represents the uniformity of this column of pixels.

Column 5, shown in Figure 5-2, also has no open apertures. However, we can see the crosstalk from Column 6. There was no crosstalk from Column 6 in Column 4. The average amplitude for this column is about 6.1 and P-P=15. Thus, the amplitude of the crosstalk is about 6% of the value of signal from a single, fully open pixel.

Column 6 (Figure 5-3) has a pattern in which 8 fully open and 8 covered pixels are repeated 8 times. The average value is 130. (P-P=150). So the variation is about ±8% over the column. Note that the tops and bottoms are not flat. The variation is about ±5% within a set of 8 pixels. The "hump" in the amplitudes is probably due to the light intensity peaking in the

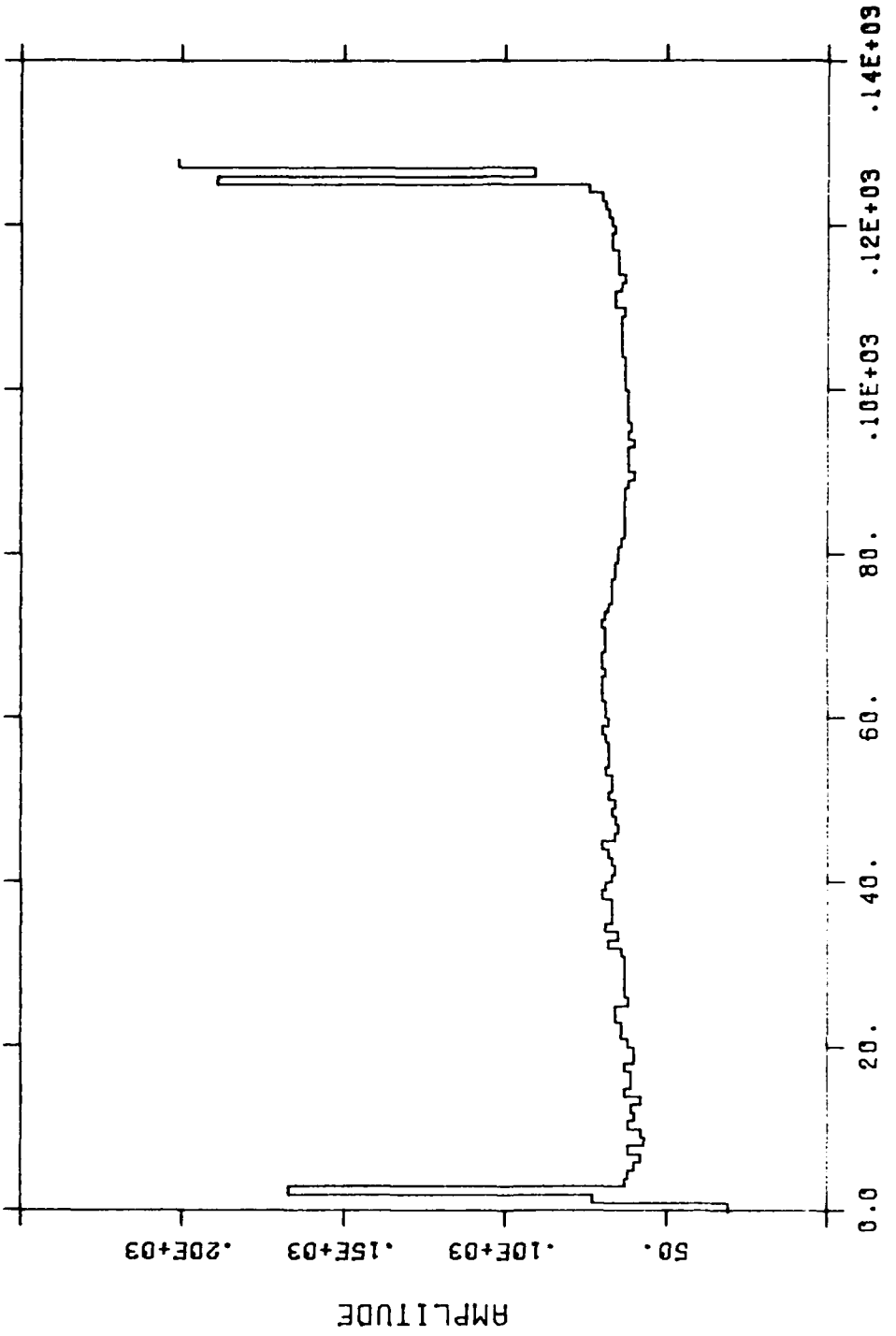


Figure 5-1. Output of CCD with test pattern mask for column 3.

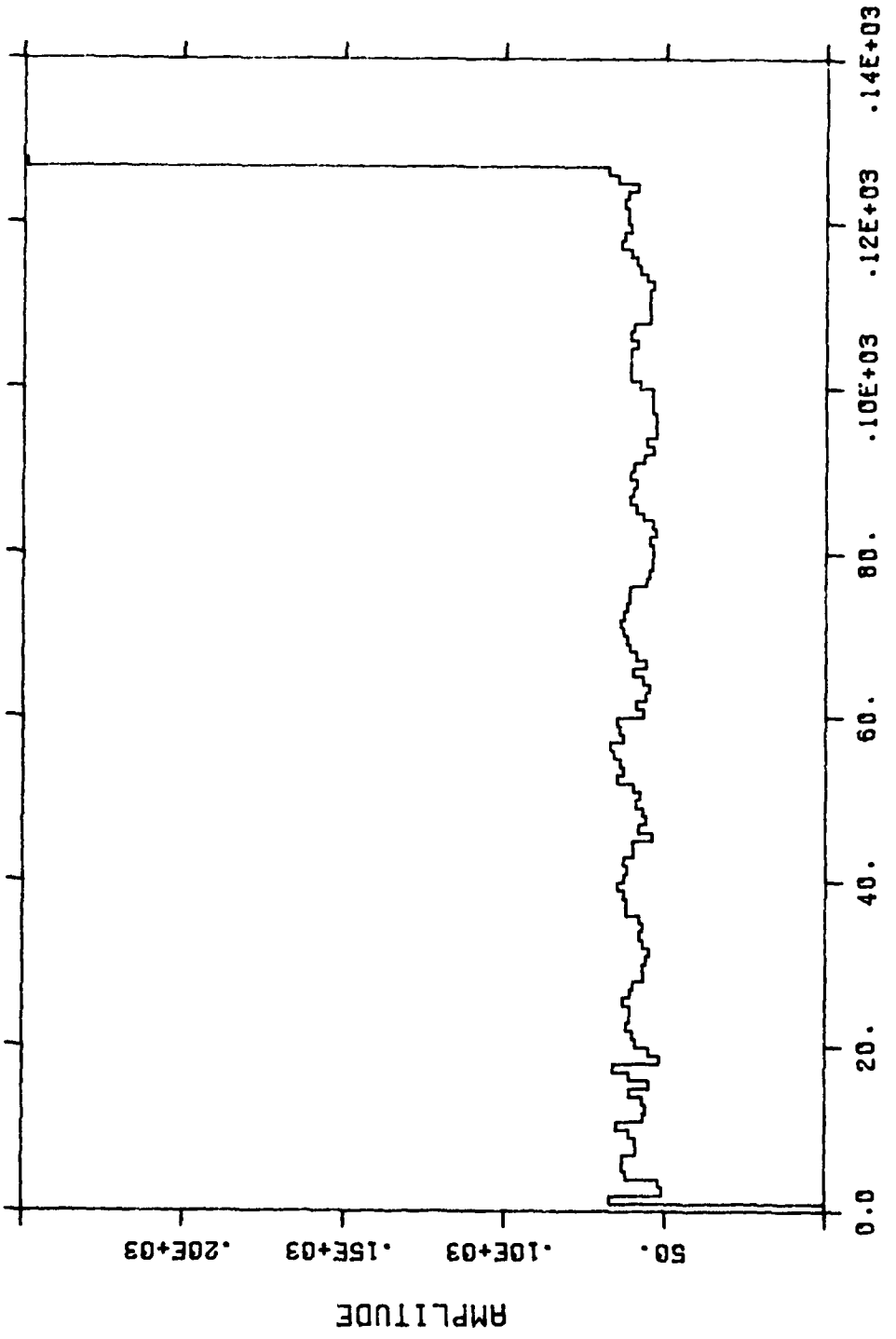


Figure 5-2. Output of CCD with test pattern mask for column 5.

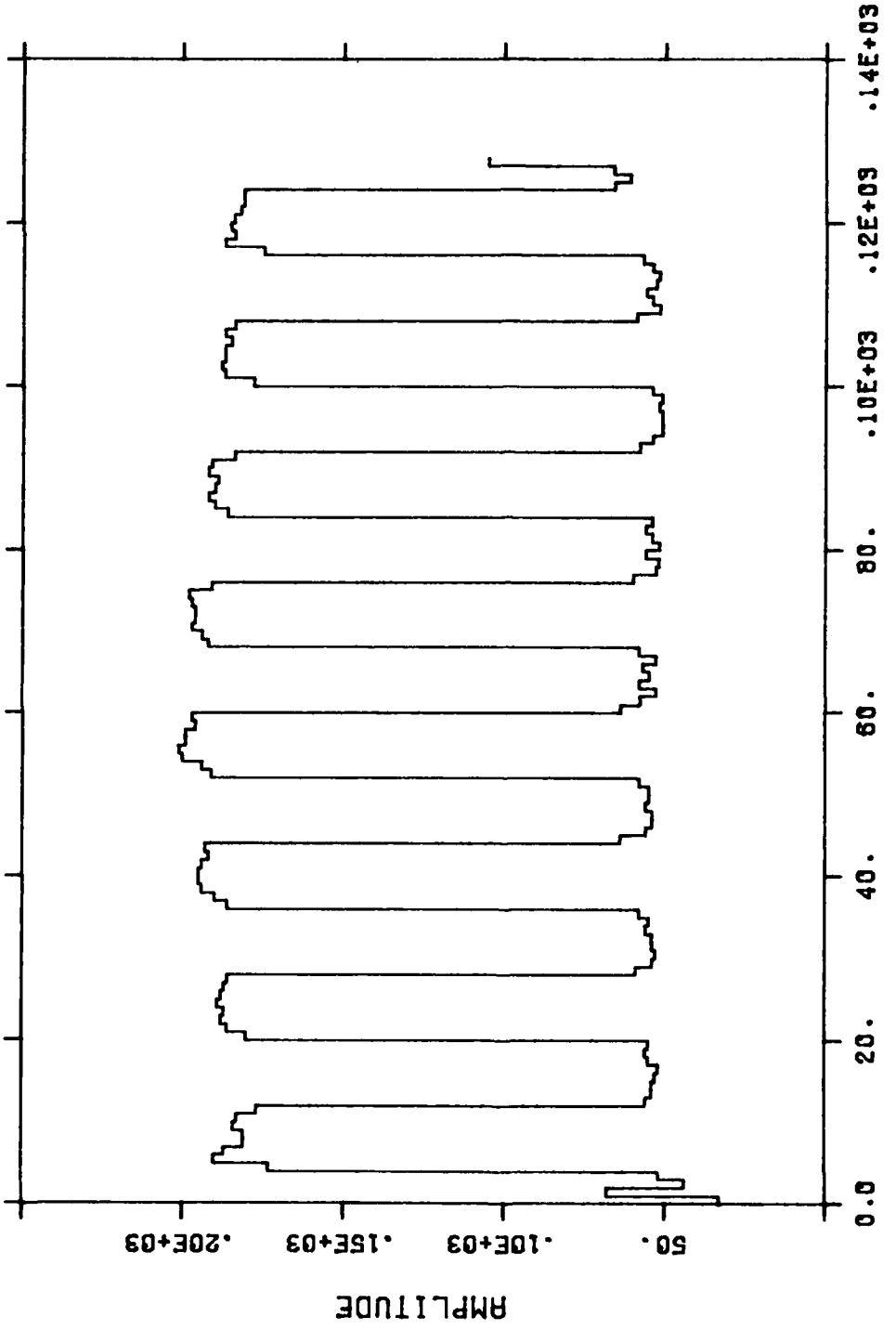


Figure 5-3. Output of CCD with test pattern mask for column 6.

middle of the array. The amplitude is about 10% larger in the center than at the edges of the array. The bottom of the square wave corresponds to empty pixels and is fairly flat.

Column 7 (Figure 5-4) shows crosstalk from both column 6 and 8. Column 8 has every other pixel fully exposed. The average amplitude is 13 with P-P=20. Note that the amplitude of the crosstalk from column 6 is about twice that which appears in column 5. This phenomenon is consistent with all columns, i.e., the column on the right has more crosstalk than the row below. The reason for this is not understood.

Column 8 (Figure 5-5) has every other pixel fully open except for the first 4 pixels and the last 4. The average amplitude is about 120. The crosstalk from column 6 is apparent. This again shows a greater crosstalk toward the right since this column is the second column from column 6 on the right and there was no noticeable crosstalk from column 6 in column 4 which is 2 columns toward the left.

Column 13 (Figure 5-6) shows some full open apertures as well as the two ramps. The ramps use only one of the two apertures per pixel. The ramp is fairly linear. The hump or curve may be partly due to the cylindrical symmetry of the illumination, i.e., more light falling on the pixels in the center portion of the column. Also, the accuracy of the apertures themselves may only be ±5% or worse.

Column 14 (Figure 5-7) has some full open apertures near the ends but only closed in the middle portion. Note the crosstalk from the ramp in column 13.

Figure 5-8 shows row 64 and column 64 which is a cross-section on two axes through the array. Note that the signal is not equal in the corners. The intensity drops from left to right while it is about equal top to bottom. It is not possible to obtain flat and equal illumination over the whole array with the present system. Measurements must be made with a best available adjustment condition. These measurements were done with row 6 optimized for flatness, since the experimental apparatus makes this the easiest parameter to view on the oscilloscope.

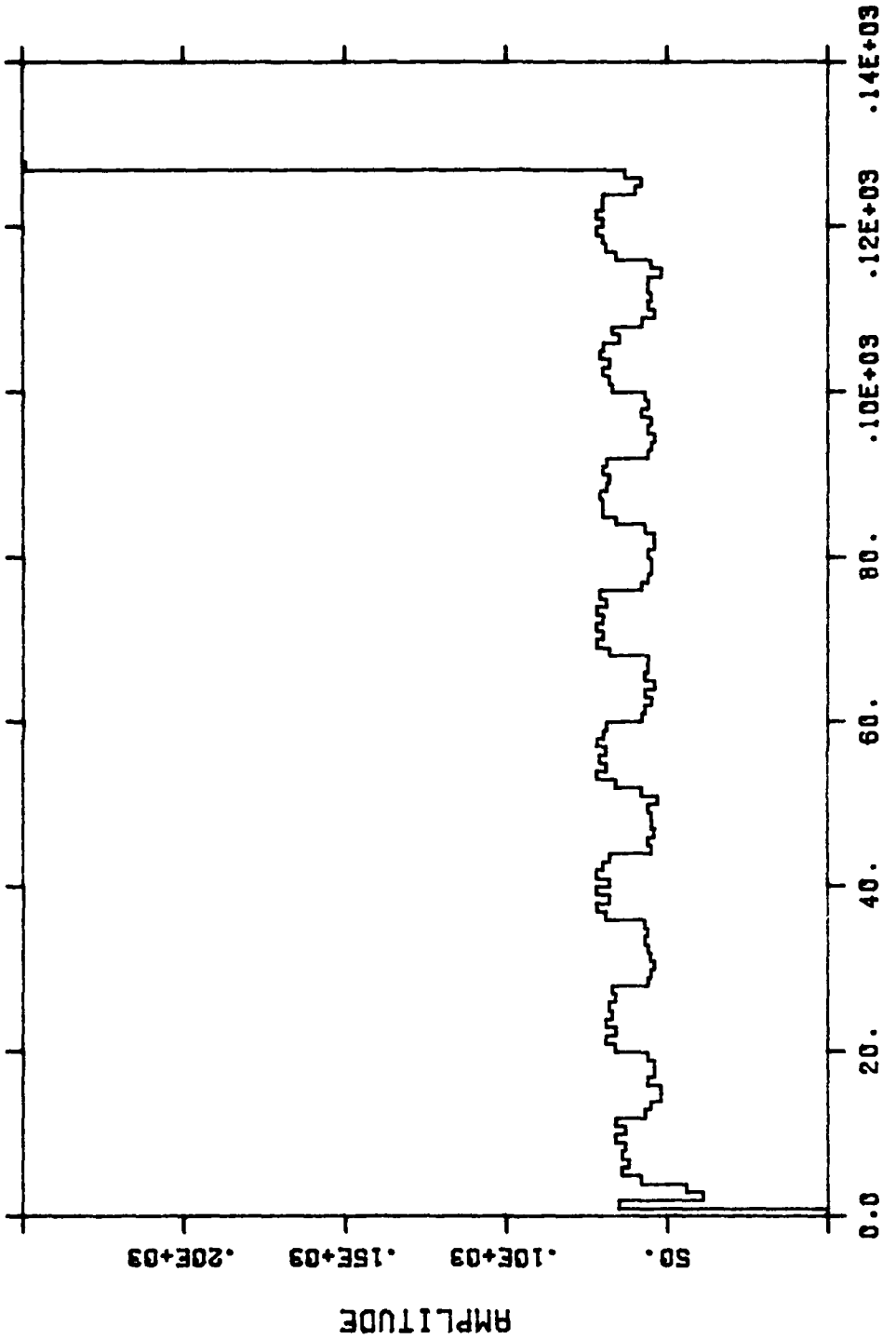


Figure 5-4. Output of CCD with test pattern mask for column 7.

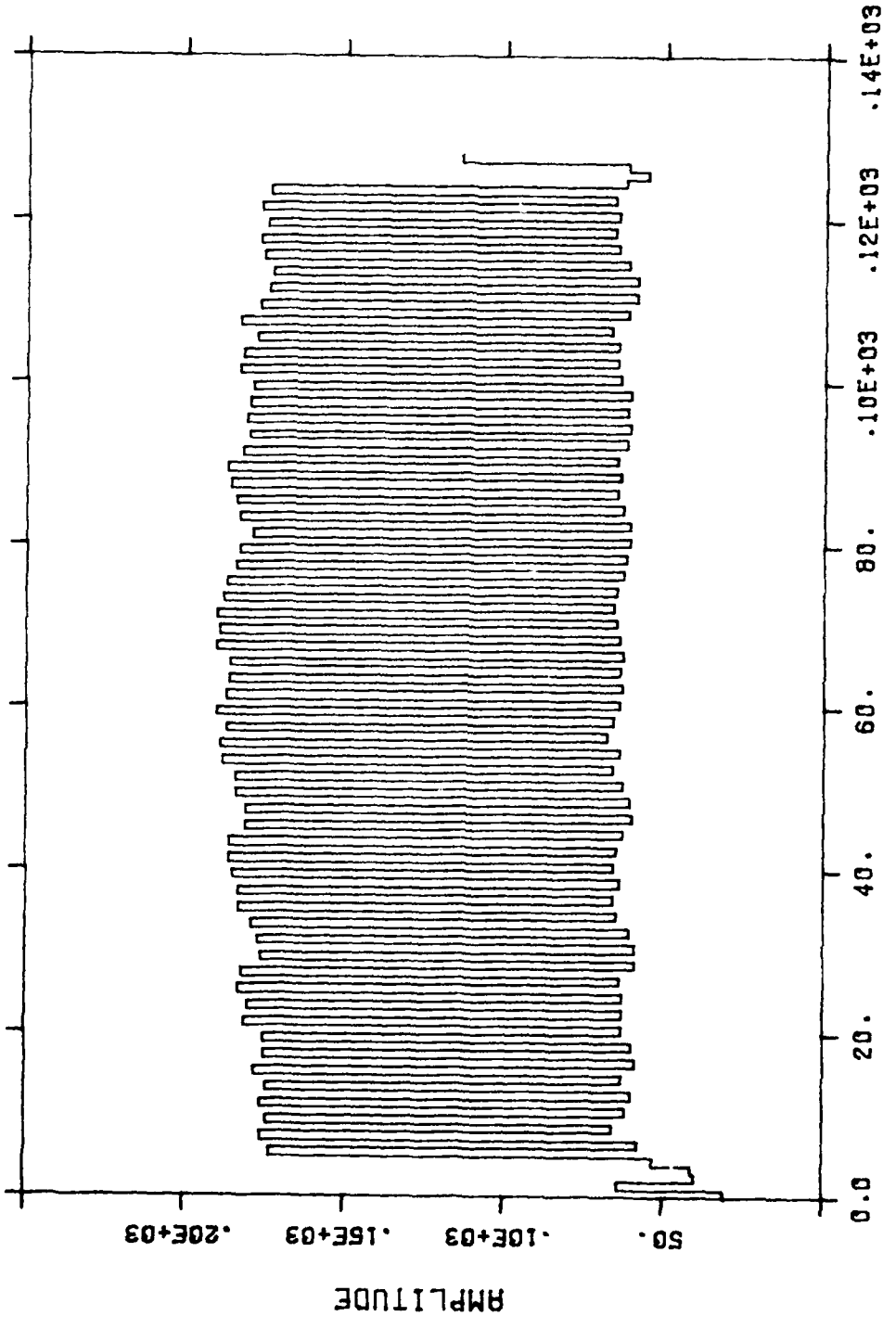


Figure 5-5. Output of CCD with test pattern mask for column 8.

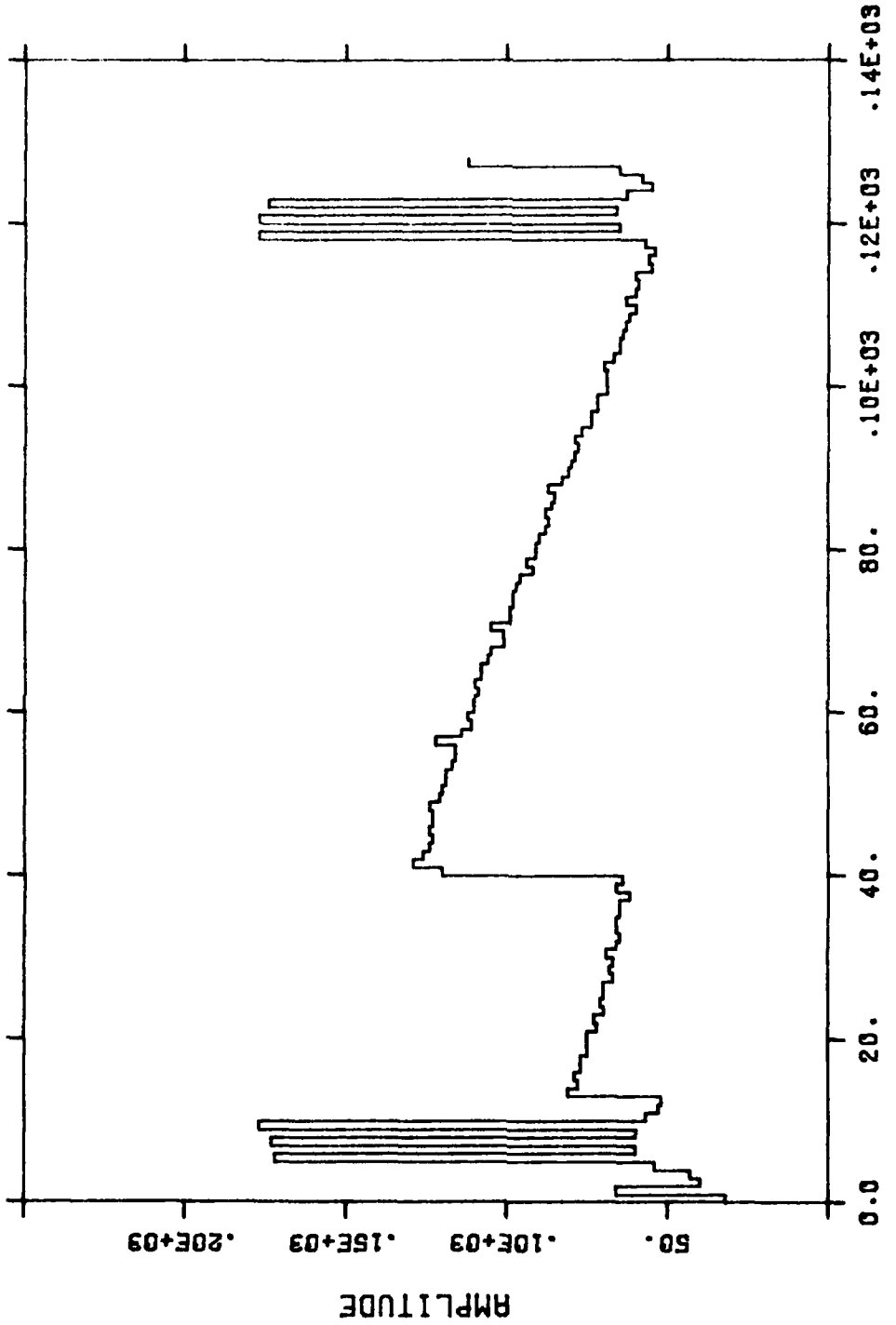


Figure 5-6. Output of CCD with test pattern mast for column 13.

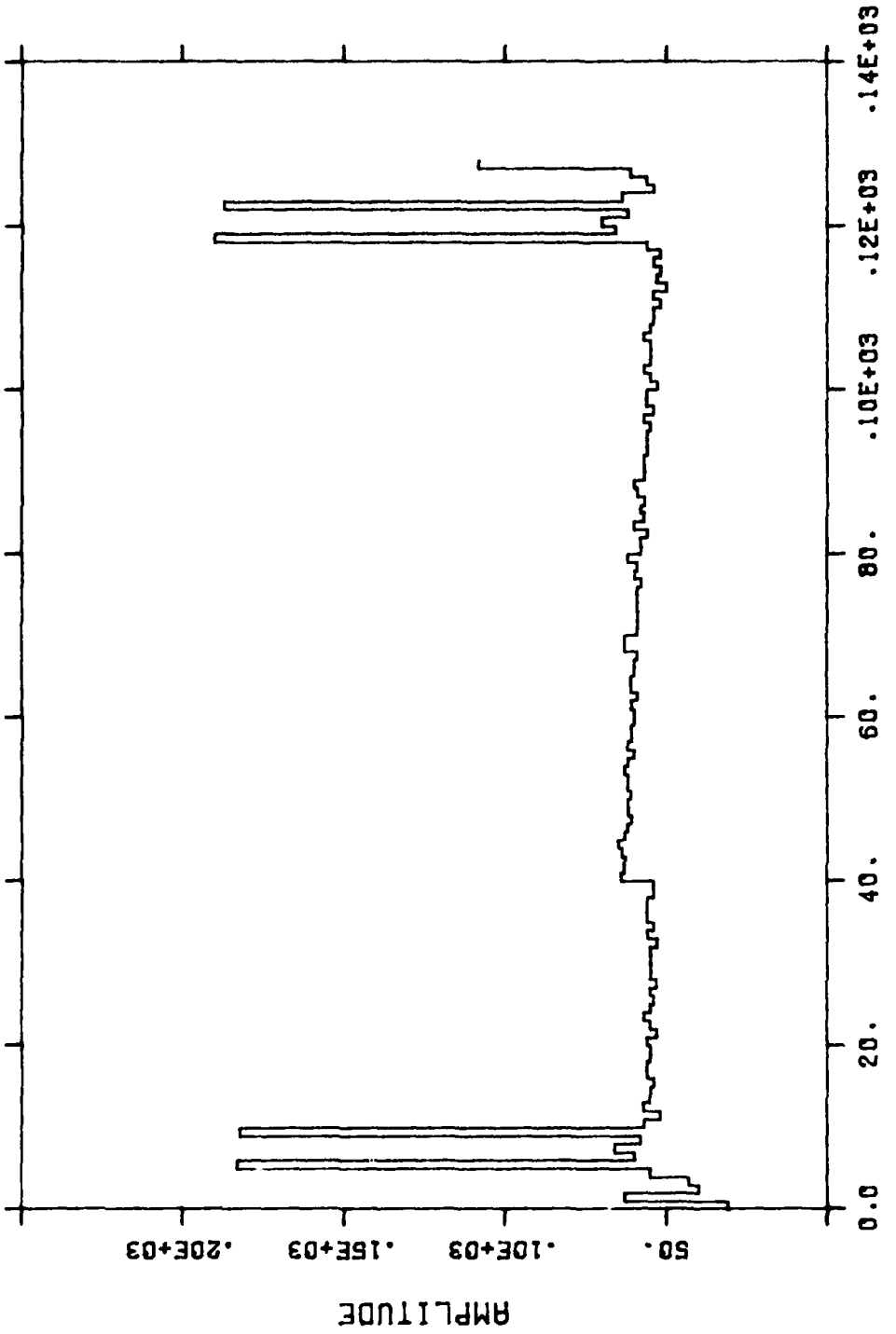


Figure 5.7. Output of CCD with test pattern mask for column 14.

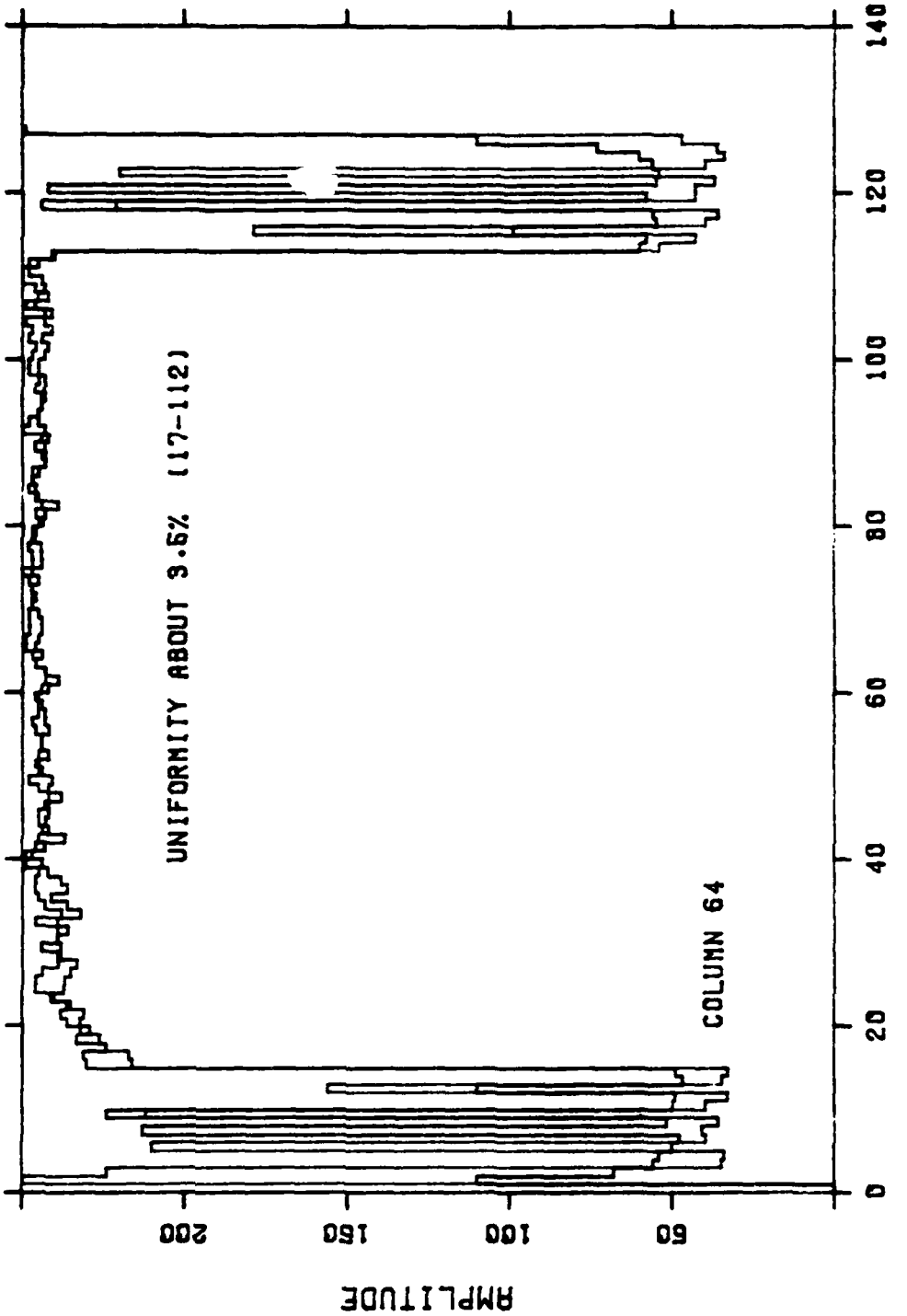


Figure 5-8. Output of CCD with test pattern mask for row 64 and column 64.

The test system described in Section 3 of this report was used to evaluate and characterize the CCD. With the implementation of simple software changes to this test system, it was also used to evaluate and characterize the CCD when used as a discrete Fourier transformer. The reader is referred to prior papers and reports for the theoretical background on the use of the electro-optic processor in performing a DFT.

Theoretically, the sum of the charge generated in each column of the CCD is constant for all columns. However, due to dimensional errors in the fabrication of the apertures, these sums may not be equal. This gives rise to a fixed noise pattern in the output of the CCD as shown in Fig. 6-1. The shape of the envelope of the fixed pattern noise waveform is mostly due to the non-uniformity of the LED intensity across the CCD.

When a 20KC square wave is applied to the LED driver, the CCD output takes on the form shown in Fig. 6-2. Note that only the more prevelant harmonics of the square wave are observable over the background fixed pattern.

When the fixed pattern noise is A/D converted, stored in the computer, and then subtracted from the output containing signal, the waveform shown in Fig. 6-3 results. The output is nearly flat and spectral components up to the 11th harmonic are easily discernable. Also, note the absence of frequency components at the second harmonic. This shows that the LED linearity is at least smaller than 2% without compensation. The small amount of residual noise is to be expected since it is close to the limit of the quantization noise in the 8-bit A/D converter. The quantization noise is seen more clearly in the trace of Fig. 6-4, where two samples of fixed pattern noise were subtracted to show typical variations in the noise pattern. Note that this does not necessarily show the noise of the EOP/DFT output, but rather the limit imposed by the choice of A/D converter.

Figure 6-5 shows the EOP output response to an arbitrary (in frequency and phase) sine wave input. Both the COS (Columns 1-64) and the SIN (Columns 64-128) components are easily resolved. This waveform represents a sinewave shifted in phase by about -45°, *i.e.* the COSINE is positive, the SINE is negative, and both amplitudes are approximately equal. The third harmonic components of the not so pure signal generator are also very prevelant.

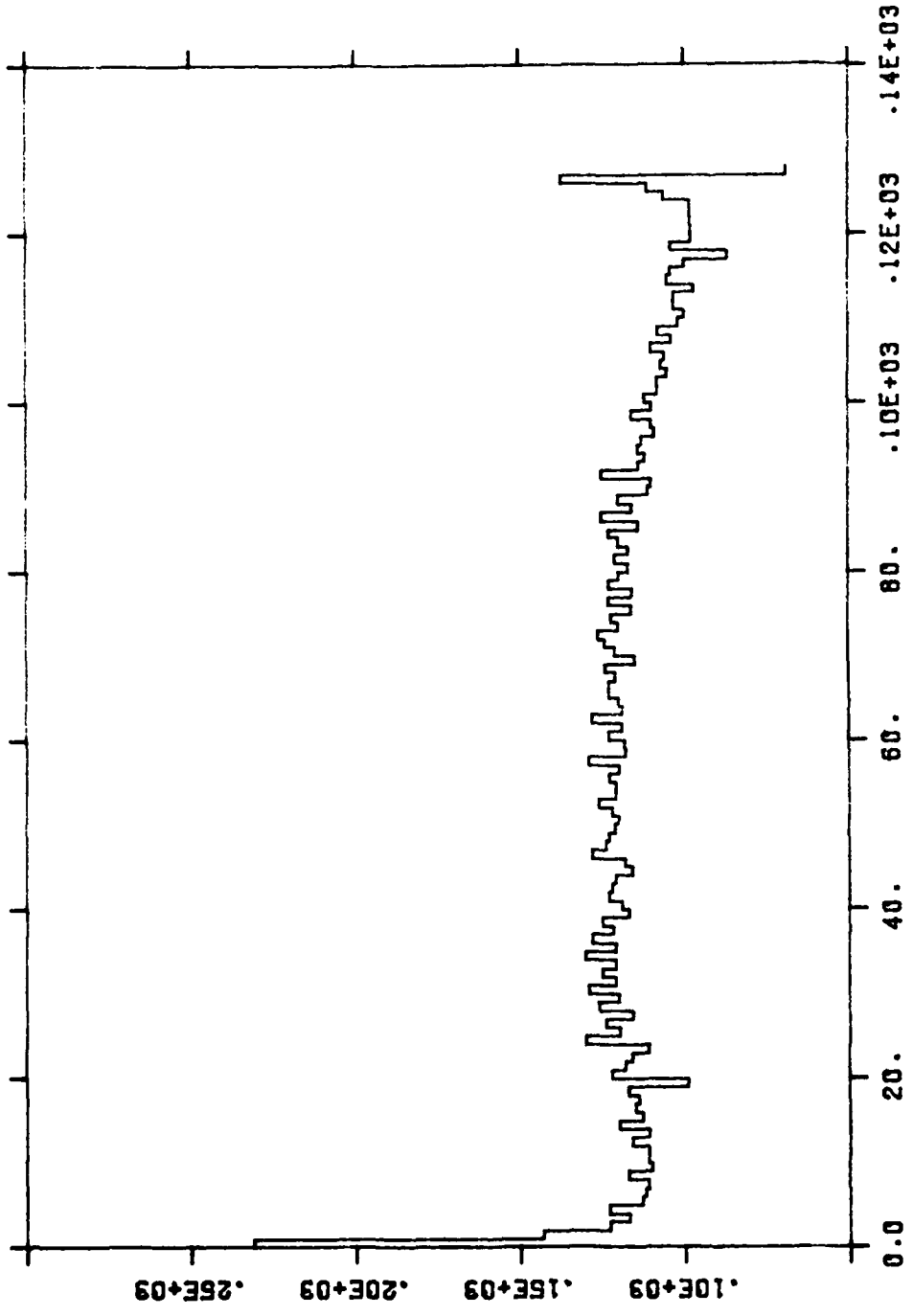


Figure 6-1. Fixed pattern noise from FOP; no signal; 640 kHz sample rate.

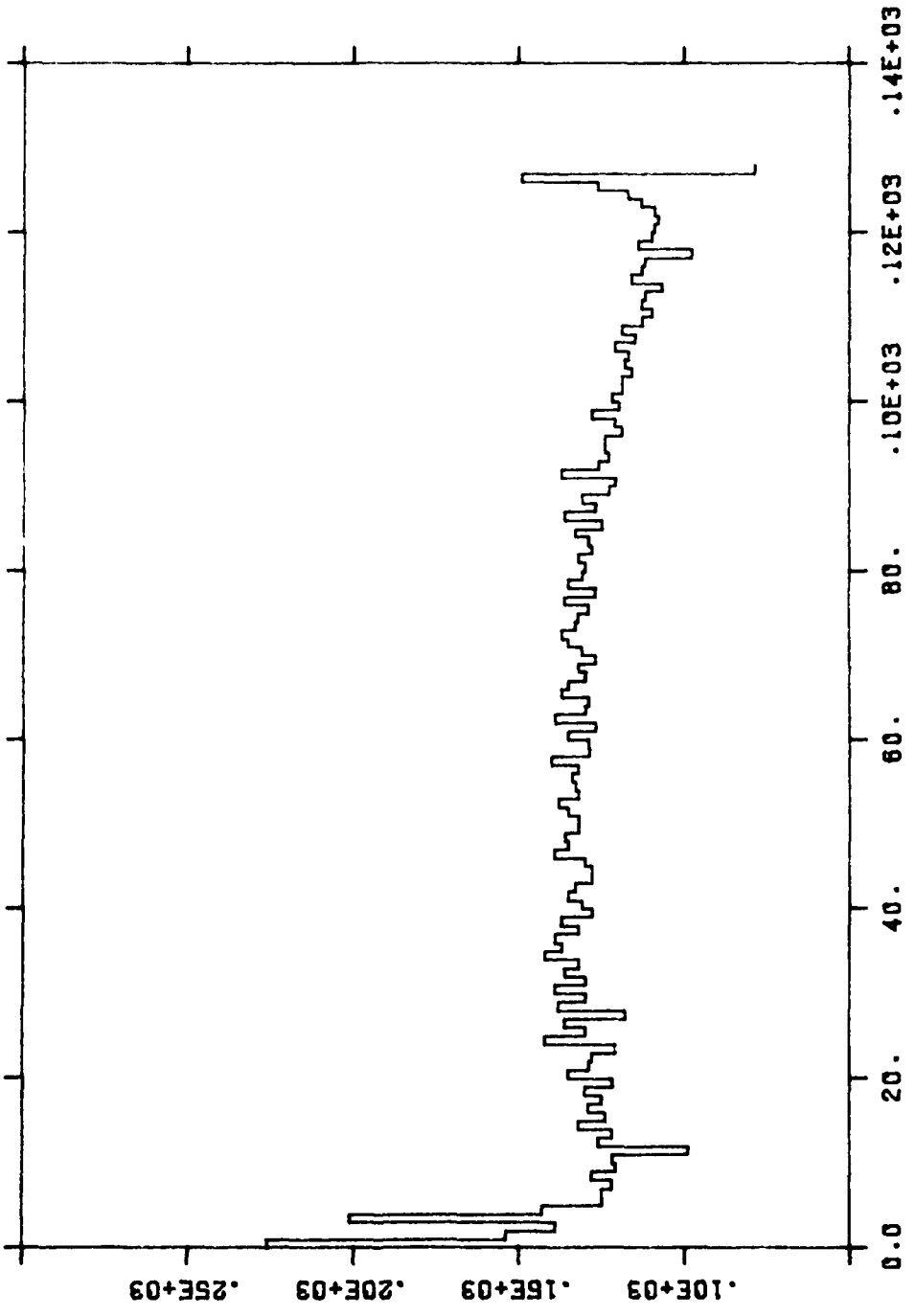


Figure 6-2. EOP output; 640 kHz sample rate, 20 kHz square wave input.

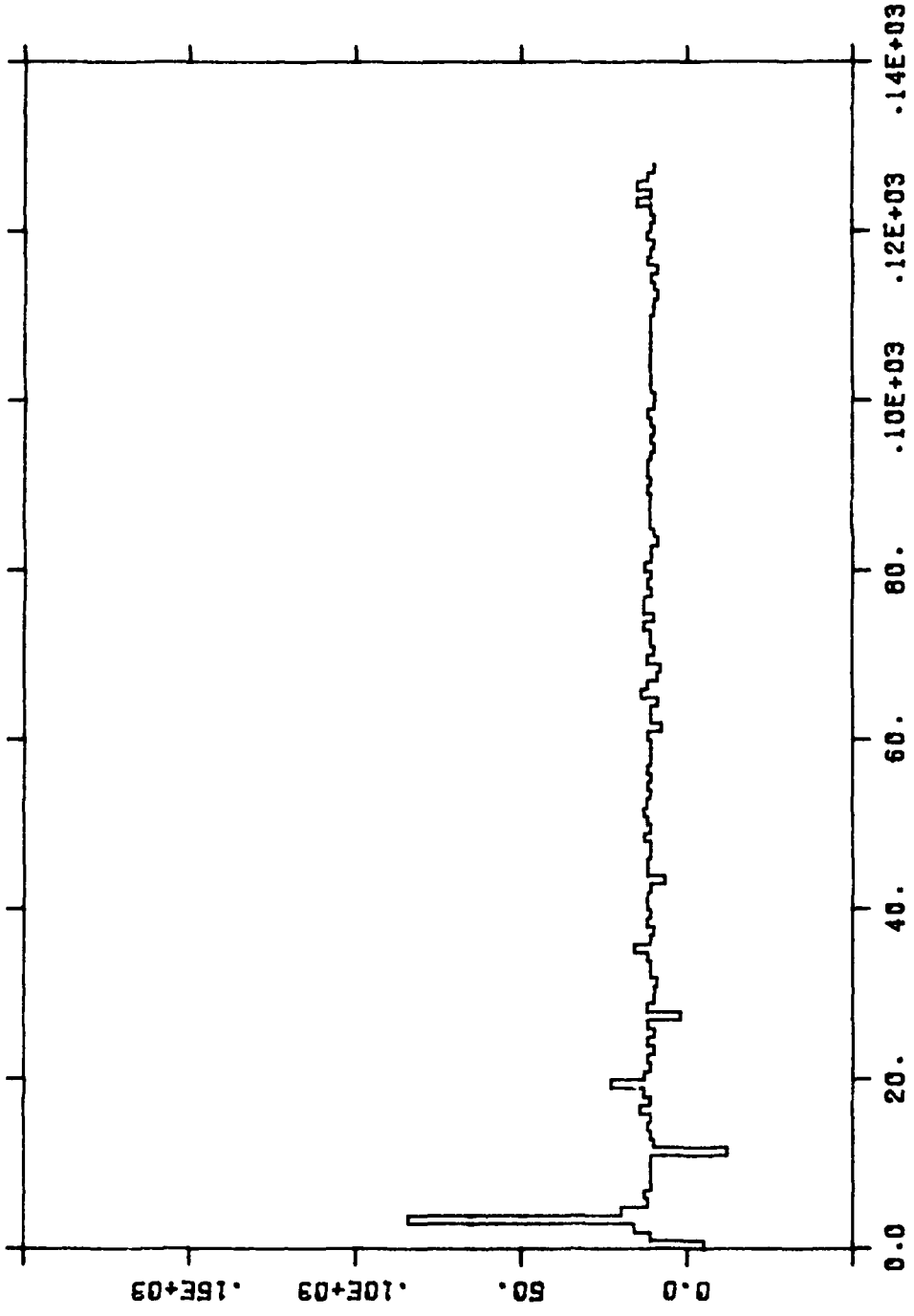


Figure 6-3. EOP output with fixed pattern subtracted; 640 kHz sample rate.

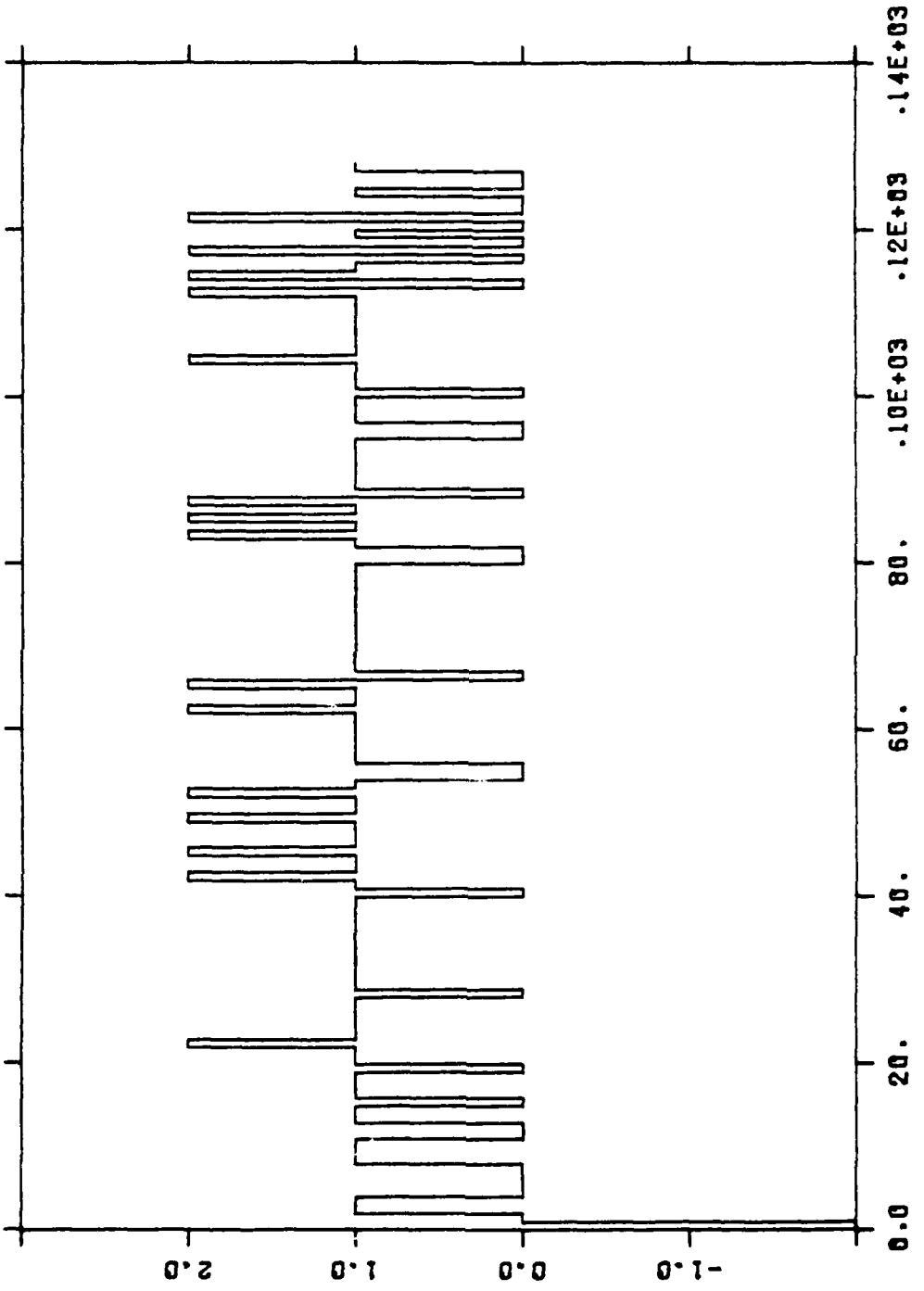


Figure 6-4. Two fixed pattern samples subtracted.

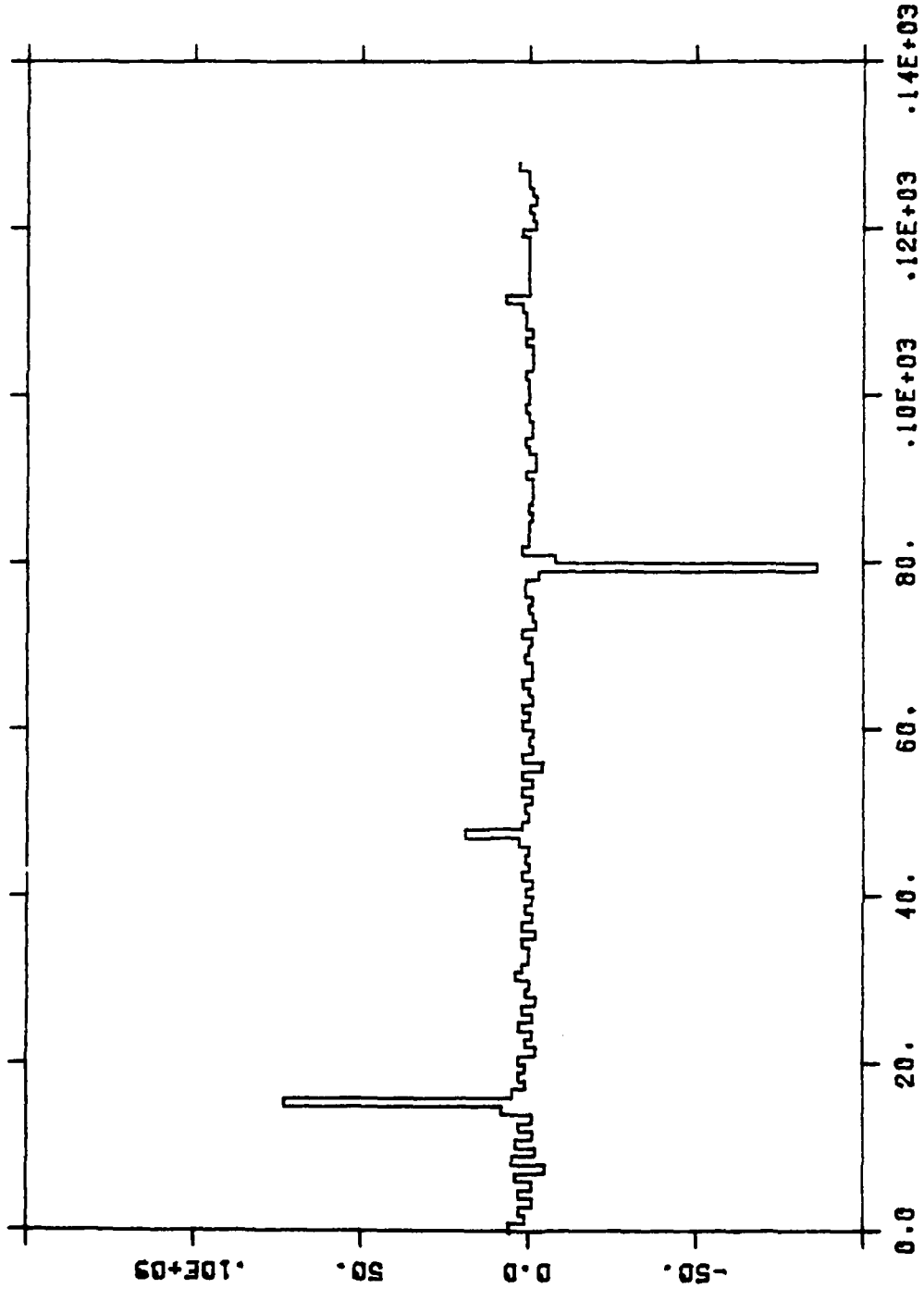


Figure 6-5. EOP output with fixed pattern subtracted frequency = 16.

REFERENCES

1. Michael A. Monahan, Keith Bromley, and Richard P. Bocker, "Incoherent Optical Correlators," Proc. IEEE, vol. 65 pp. 121-129, January 1977.

2. Keith Bromley, Michael A. Monahan, Richard P. Bocker, Anthony C. H. Louie, and Richard D. Martin, "Incoherent Optical Signal Processing Using Charge-Coupled Devices (CCD's)," SPIE vol. 118 - Optical Signal and Information Processing (IOCC 1977), pp. 118-123.

3. Anthony C. H. Louie, Keith Bromley, Thomas E. Keenan, "The EOP - A CCD-Based Electrooptical Processor," Proceedings of the 1978 International Conference on the Application of Charge Coupled Devices, San Diego, CA, 25-27 October 1978.

4. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of CCD's," RCA Review 36, pp. 577-579, 1975 (Sept.)

5. L. Jastrzebski, P. A. Levine, W. A. Fisher, A. D. Cope, E.D. Savoye, and W. N. Henry, "Origin of Localized Defects in CCD Imagers," 157th Meeting of Electro-Chemical Society, St. Louis, May 11-16, 1980.

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